SYNCHRONIZED CLOCK
MODEL 8171A

INSTRUCTION MANUAL

PLEASE NOTE OUR NEW ADDRESS

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WARRANTY

Spectracom Corporation warrants to the original purchaser each new instrument to be free from defects in material and workmanship for a period of one year after shipment. Repair or replacement, at our option, will be made when our examination indicates that defects are due to workmanship or materials. Electron tubes, batteries, fuses, and lamps that have given normal service are excluded from warranty coverage. All warranty returns must first be authorized in writing by the factory.

This warranty does not apply to any of our products which have been repaired or altered by persons not authorized by Spectracom Corp. or not in accordance with instructions furnished by us. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, or if any serial number or seal has been removed or altered, the warranty is void and repairs will be billed at cost.

This warranty is in lieu of all other obligations or liabilities expressed or implied and Spectracom Corp. neither assumes nor authorizes any person to assume for them, any other liability in connection with sales of its products.

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Instruments should be returned only upon prior written authorization from Spectracom Corp. or its authorized sales and service representative. Warranty repair will be made upon written request. Please provide the following information in order to enable us to serve you efficiently:

1. Model Number and type
2. Serial Number
3. Description of trouble
4. Conditions and hours of use

Upon receipt of this information our service department will send you service data or shipping instructions. Transportation to the factory is to be prepaid by the purchaser.

For assistance contact your nearest Spectracom sales representative.

WARRANTY REGISTRATION

Spectracom Corporation
95 Methodist Hill Dr. Ste 500
Rochester, NY 14623

Dear Customer,

Spectracom occasionally contacts customers regarding our products. We must know to whom we should send manual updates, change notices, and new product information. Because people sometimes change job assignments, we request department, mail station, and title information to ensure that correspondence in future years will reach either the user of our products or his/her supervisor. In filling out the registration, please use the title/mail station/department of the supervisor most interested in keeping the equipment and its documentation up-to-date. Thank you.

- -

Name _____ Title _____

Department _____ Mail Stop _____

Company _____ Model Number _____

Address _____ Serial No. _____

City _____ Date Installed _____

State_____ Zip _____

Telephone_____ Ext. _____

Remarks (problems, suggestions, etc.): _____

_____

_____

_____

_____

CERTIFICATE OF TRACEABILITY

SPECTRACOM CORPORATION hereby certifies that its Model 8171A Synchronized Clock provides direct traceability to the National Bureau of Standards, when operated in conjuction with a Spectracom WWVB Receiver with time code output.

When properly installed and maintained, the Model 8171A provides time accuracy and output resolution as published in the equipment's instruction manual.

SPECTRACOM CORPORATION

IMPORTANT INSTALLATION NOTICE

The Model 8171A operates in conjunction with a WWVB receiver (Models 8160A, 8161, or 8164). Data is transmitted via an RS-422 bus. The cable must be terminated at both ends in it's characteristic impedance.

To accomplish this, connect a terminator plug (Spectracom Part Number 015504) to the BUS A connector of the Model 8171A unit which is connected to a WWVB reciever. This termination is required even if only one Model 8171A unit is utilized.

If additional Model 8171A units are to be daisy-chained to the first 8171A unit's bus, connect a terminator receptacle (Spectracom Part Number 015505) to BUS B of the last Model 8171A in the chain.

For further details, refer to Section 1.2.9, and Figure 1-3 of this manual.

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SECTION 1

8171A

INSTALLATION & OPERATION

1.1 INTRODUCTION

The Spectracom Model 8171A Synchronized Clock decodes the time signal output of a Model 8160A, 8161, or 8164 WWVB Receiver/Frequency Standard, and provides a front panel display of hours, minutes, and seconds. A serial RS-232C interface provides on command: day of the year, hours, minutes, seconds, time zone and status information. A 1-Hz on-time pulse that signals the beginning of each second is available on the rear panel. A thumbwheel switch on the rear panel provides for time zone, daylight saving time, and path delay corrections. Several Model 8171 units may be "daisy-chained" together and connected to the output of a single WWVB Receiver/Frequency Standard.

Output data options include:

Option 18, Parallel BCD Output
Option 19, Remote Output (RS-422,RS-232). Option 19 is standard on units with serial numbers 8171-0566 and higher.
Option 23, IRIG B Output
Option 30, Fully Decoded Text Stream

Other options available are:

Option 01, Rack Mount Kit
Option 11, Rack Mount with Slides
Option 24, TCXO Stand-by oscillator

1.2. INSTALLATION

1.2.1 UNPACKING

In the event of damage to the shipping carton or if there is hidden damage inside but the carton is not damaged, be sure to contact the carrier immediately so that his representative can witness any equipment damage that may exist inside the carton. If you fail to report shipping damage immediately you may forfeit any claim against the carrier. You should also notify Spectracom Corporation of shipping damages so that we can assist you in obtaining a replacement or repair the equipment.

Be sure to remove all items of equipment and accessories from the shipping carton before discarding it. This includes a three-conductor line cord, an instruction manual, and an ancillary kit.

1.2.2 RESHIPMENT

If it is necessary to return the unit to the factory, the original shipping carton may be used. If it is not available, a carton of at least 250# test corrugated paper with at least two inches of polyethylene foam surrounding the unit must be used. The unit should be sealed in a plastic bag for moisture protection and a note must be included stating the reason for the return.

1.2.3 INPUT POWER

The equipment may be operated from 115 VAC ±10%, 50/60-Hz line power.

1.2.4 OPERATING ENVIRONMENT

The equipment is designed for operation in a room temperature laboratory environment. Operation outside a temperature range of 0 to 50°C may cause malfunction or damage to the equipment.

1.2.5 BENCH OPERATION

The instrument is provided with four feet for standing on a benchtop surface, along with a tilt stand which may be used to provide a convenient viewing angle.

1.2.6 RACK MOUNT KIT (Option 01)

Units purchased with the rack mount kit are not provided with the tilt stand. The four mounting feet are included but these may be removed when the receiver is installed in a rack.

The rack mount panel extensions are installed by removing the vinyl-covered filler panels located just behind the handles on the sides of the enclosure. The rack mounting brackets are installed using the oval head #10-32 x 3/8 screws provided. Truss head #10-32 x 3/8 screws are furnished to mount the unit to the rack. (See Figure 1-1)

1.2.7 RACK MOUNT WITH SLIDES (Option 11)

The chassis section of the slides are attached to the sides of the receiver using the #10-32 x 3/4 screws provided. The filler plates are located between the slides and the receiver sides.

The stationary section of each rack slide must be assembled to the proper length for the rack being used, using the brackets, screws, and nuts provided. The slides are bolted to the front and rear channels of the rack using the #10-32 x 1/2 screws and nut plates as shown in Figure 1-2. Additional panel mounting angles (such as Emcor No. PMA) may be added to the rack cabinet for securing the front ends of the stationary slide sections if needed. They should be located immediately behind the panel mounting angles to which the equipment panel extensions will be fastened.

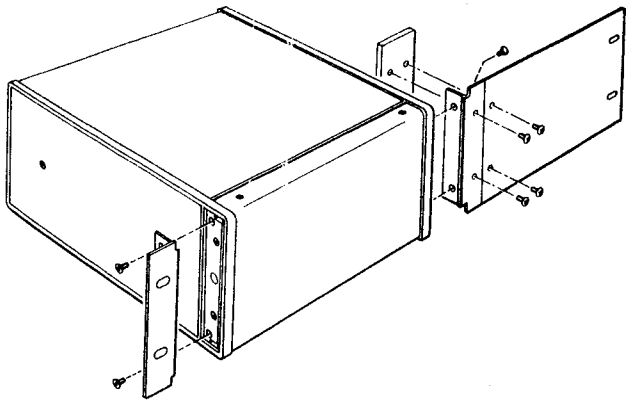


FIG. 1-1 RACK MOUNT OPTION 01

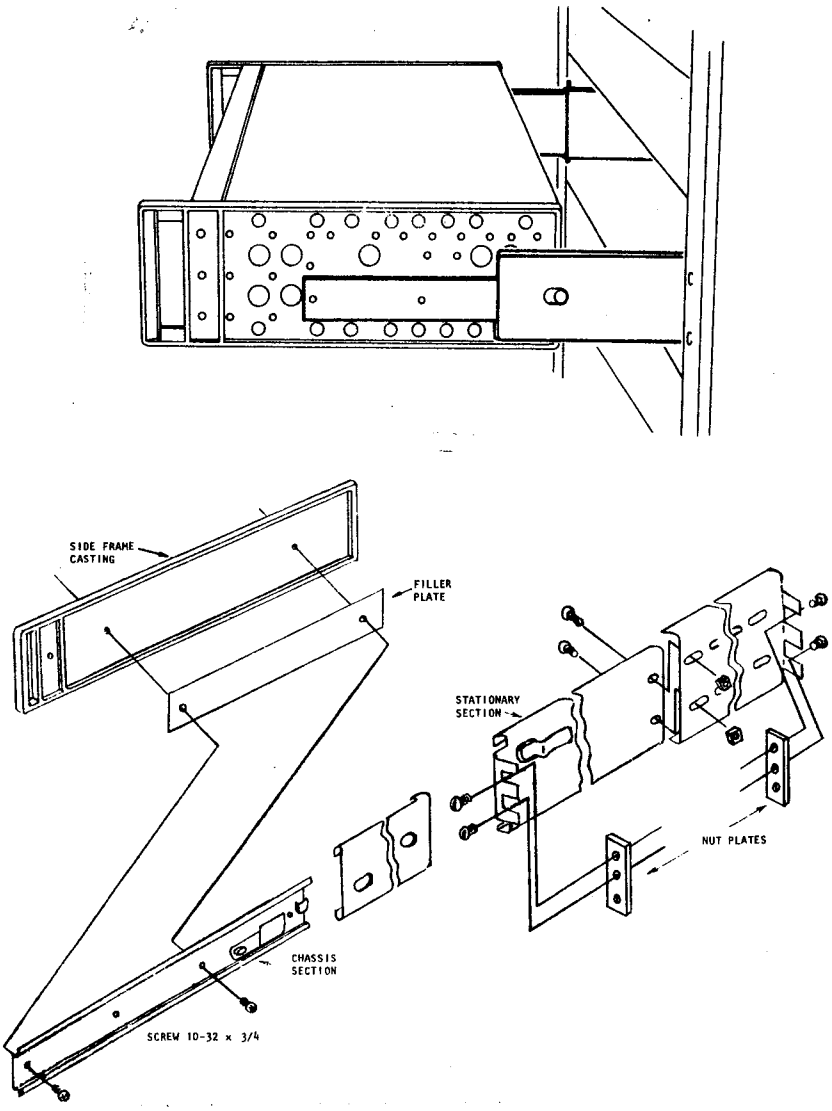


FIG. 1-2 RACK MOUNT WITH SLIDES (OPTION 11)

1.2.8 INTERNAL SWITCHES

Refer to Figure 2-3 for physical location of internal switches.

The switch functions are listed below. The switch is present only if the Option is present.

SW1	Option 30	Select year - units position
SW2	Standard	Selectable Bit Rate
SW3	Option 30	Select year - tens position
SW4-1	Option 23	IRIG B Control Function
-2	Option 30	Select Option 30
-3	Standard	Time Sync LED Time Out
-4	Standard	Time Sync LED Time Out
SW5	Option 23	IRIG Code Select
SW6	Option 23	IRIG TTL/AM Output Select

The standard unit contains the following switches. They are set at the factory to the positions indicated below:

SWITCH	SET	DESCRIPTION
SW2	2	Selectable Bit Rate set to 300 baud
SW4-1	X	X - don't care
-2	OFF	Option 30 not present
-3	ON)	Time Sync Time Out set
-4	ON)	for 3 hours

Switch (SW2) located on the microprocessor assembly A1A2 is a 10-position switch which controls the bit rate of the serial I/0 port. The table below lists the bit rate as a function of the switch setting.

Switch Position	**Bit Rate**
0	75
1	150
2	300
3	600
4	1200
5	2400
6	4800
7	9600
8	19200
9	110

If Option 18 Parallel BCD and Option 23 IRIG B are present, then switch SW4-1 is set OFF (open) and data is sent out the parallel BCD connector.

If Option 23 IRIG B is present, then SW5 is set to position 2, IRIG B select and SW6 is set ON - TTL output.

If Option 30, Fully Decoded Text Stream is present, then SW3 and SW1 are set to the last two digits of the current year (i.e. 84).

Refer to Section 4.0 Options for a detailed description of switches associated with each system.

1.2.9 CONNECTION AS PART OF A SYSTEM

The Model 8171A Synchronized Clock is driven by the time code output (Option 05) of a Model 8160A, 8161, or 8164. Figure 1-3, System Configuration, illustrates how several Synchronized Clock units may be connected in a "daisy-chain" to one receiver output. The AUX IN/OUT connector on the rear panel of the Receiver is connected by means of Cable A to the AUX connector on the rear panel of the first synchronized clock in the chain. Additional synchronized clocks are connected into the system using a Cable B from the Bus B connector on the rear panel of each synchronized clock to the Bus A connector on the next unit in the chain. The last unit in the chain must have a Bus Terminator connected to its Bus B connector. Similarly, the first unit must have a terminator connected to its Bus A connector. Cable B has a female connector for mating with the Bus B connector on the synchronized clock and a male connector for mating with the Bus A connector. Consequently, if a synchronized clock is removed from the chain, the two Cable B's connected to it may be connected to each other.

Note: A bus terminator assembly is required at each end of the RS-422 time distribution bus as shown in figure 1-3 below. Terminating the cable ends preserves data integrity by preventing signal reflections and oscillations.

Terminate the Bus A connector with Bus Terminator part number 015504. This terminator is required even if only one Model 8171A unit is utilized. If additional Model 8171A units are to be daisy-chained to the first 8171A unit's bus, connect the Bus B terminator part number 015505 to the last Model 8171A in the chain.

Failing to terminate the RS-422 time data bus may cause one or all the Model 8171A in the chain to display and output the incorrect time even though the front panel Time Sync lamp is illuminated.

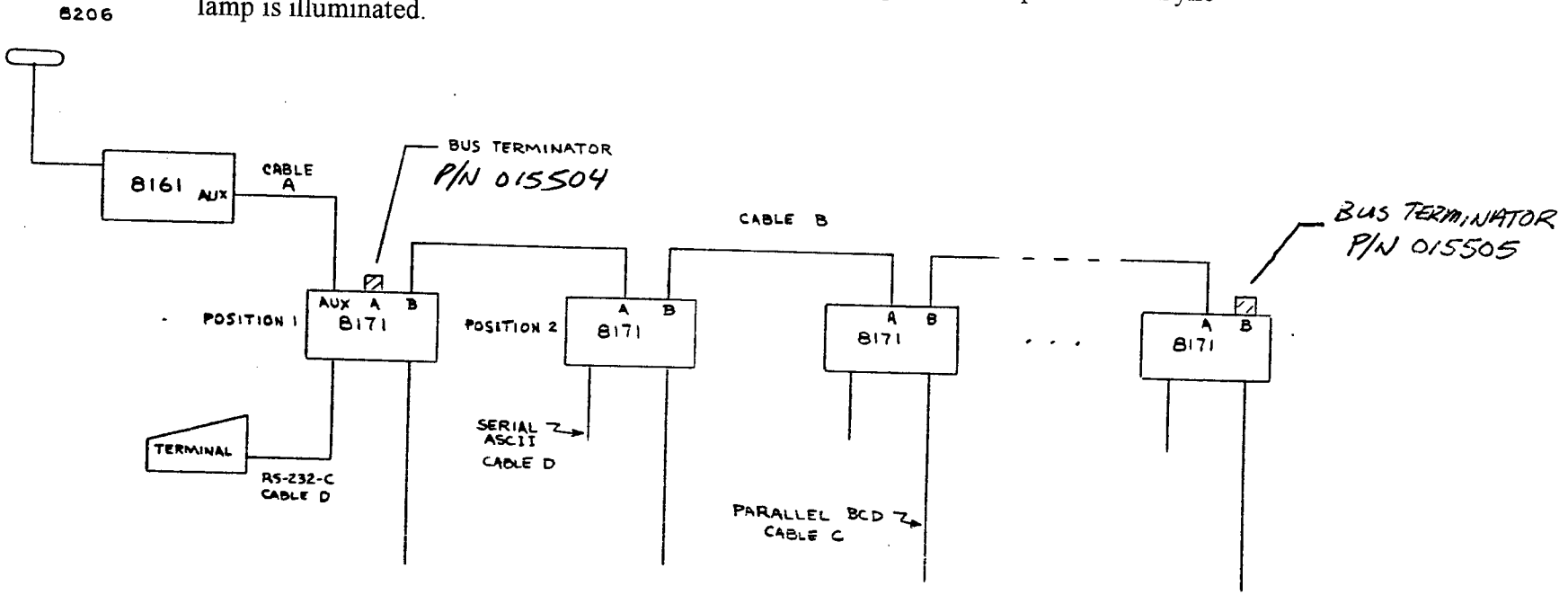


FIG. 1-3 SYSTEM CONFIGURATION

1.2.10 MATING CONNECTORS & CABLES AND TERMINATORS

The mating connectors for the rear panel are listed below. The pin numbers for each signal are listed in Paragraph 1.4.3 of this section. Equivalent connectors may be substituted.

REFERENCE	DESIGNATION	MFR. PART NO.
AUX IN/OUT	Plug, 15 Circuits	Molex 03-09-2151
	Pin	Molex 02-09-2118
Serial ASCII	Plug, 25 Circuits	AMP 205208-1
	Pin for 24-28 AWG wire	AMP 66507-8
	Shell	AMP 206478-3
Bus B	Receptacle, 14 Circuits	AMP 552312-1
	Strain Relief Cover	AMP 2-552079-1
Bus A	Plug, 14 Circuits	AMP 552282-2
	Strain Relief Cover	AMP 2-552079-1
Parallel BCD	Plug, 50 Circuits	AMP 229974-1
	Strain Relief Cover	AMP 4-552008-1
Remote Output (Option 19)	Plug, 9 position	AMP 205204-1
	*Socket Pins	AMP 66506-8
	Shell	AMP 206478-1

* The crimping tool for the pins is AMP 90302-1. The insertion/extractor tool is AMP 91067-2.

Cable assemblies and bus terminators are listed below:

CABLE A	Cable with male Molex connector at each end. Cable consists of three coaxial cables.	Spectracom CA06XXX (XXX = cable length)
CABLE B	RS-422 cable with 14-pin male Champ connector at one end and 14-pin female Champ connector at other.	Spectracom CA07XXX (XXX = cable length)
TERMINATOR	120-ohm Bus terminator housed in 14-pin Champ connector plug housing. Plugs into Bus A.	Spectracom 015504
TERMINATOR	120-ohm Bus terminator housed in 14-pin Champ connector receptacle housing. Plugs into Bus B.	Spectracom 015505

1.3 OPERATION

1.3.1 FRONT PANEL FUNCTIONS

Time Sync: The green lamp is turned on when the time code is fully decoded. In order to select the length of time before the time sync lamp goes out after loss of phase lock, switch (SW4-3,4) can be set to select 1 of 4 times:

SW4-4 Setting	SW4-3 Setting	Time (min)	Typical Error (msec)
0	0	10	1
0	1	20	10
1	0	60	30
1	1	180	100

The lamp will come back on after the receiver reacquires phase lock to the WWVB carrier and the time code is decoded.

If high accuracy during loss of signal is required then Option 24 TCXO and External Oscillator is recommended. Refer to Section 4 - Options for details.

Display: The display initially indicates time since "power on" in the four right hand digits. After the Receiver/Frequency Standard acquires phase lock the sixth (left most) digit displays the code received. (See Figure 1-5, WWVB Time Code Format). A zero (0) is a logical zero, a one (1) is a logical one, a two (2) is a position identifier and a four (4) indicates a bit error. After the code is successfully received universal coordinated time (UTC) minus the time zone switch setting is displayed.

1.3.2 REAR PANEL FUNCTIONS

Thumbwheel Switch: This is a 5-digit switch. The right two digits are TIME ZONE. The left three digits are PROPAGATION DELAY and RECEIVER DELAY inputs. The propagation delay can be calculated (see Section 1.3.8 PROPAGATION PATH DELAY). The receiver delay is nominally 17 milliseconds. Set the switch to the sum of the path delay and receiver delay.

Daylight Savings Time: Use the TIME ZONE switch to adjust the display for local time.

Parallel BCD: Option 18 provides the day of the year, hours, minutes, seconds, time zone and status data on a 50-pin connector.

Remote Output Driver: Option 19 provides a RS-422 serial data output for driving Model 8172 Synchronized Wall Clocks or Model 8173 Multiple RS-232C Taps.

IRIG B Output: Option 23 provides 1-KHz carrier, amplitude modulated at 100 pps with time code or 100 pps DC level shift.

External Oscillator Input: Option 24 rear panel BNC input for 1.0-MHz standby clock oscillator.

Serial ASCII: This interface is a serial RS-232C port. The connector is a 25-pin series D socket.

There are 3 commands:
S - Set the clock
T - Read the time
D - Dump the memory

Power: International Electrotechnical Commission (IEC) male line cord receptacle.

Line Fuse: AC line fuse. AGC 3/4 A.

AUX: Input signal connector provides Receiver/Frequency Standard output signals to the first Model 8171 Synchronized Clock in the chain.

BUS A: Input signal connector provides inputs to Synchronized Clock units other than the first in the chain. A bus terminator is connected to the BUS A connector on the first unit of the chain.

BUS B: Output signal connector provides Receiver/Frequency Standard signals to the next Synchronized Clock in the chain. A bus terminator is connected to the BUS B connector on the last unit of the chain.

1.3.3 INITIAL TURN-ON

After the Model 8171A Synchronized Clock has been connected into the system as described above, plug it into the power line. The Model 8164, 8161 or 8160A Receiver should be turned on and operating. The Synchronized Clock will display the time since it was turned on in minutes and seconds. After the Receiver achieves phase lock the received time code will be displayed in the left-most significant digit position, as received at one bit per second.

The time code displayed in the left digit is coded:

0 - binary zero
1 - binary one
2 - position identifier
4 - bit error

The clock receives the code and sets itself automatically. The time it takes to set is dependent on the quality of the signal received. The quality of the signal is indicated by the code received. If many 4's are displayed, then the signal is poor. If the signal is good, then the clock will set in a few minutes. If there is a weak or noisy signal, it will take longer to set.

1.3.4 COMMANDS

Commands are accepted through the Serial ASCII port. Commands are:

T - print the Time
S - Set the time
D - Dump the memory

Commands are not echoed back. Do not enter Return after the command.

Serial Data Interface:

RS-232 Port: Standard in all units, provides day and time in response to a "T" input command. "S" command allows operator to set clock via a data terminal keyboard. "D" command causes a memory dump of statistical data for performance evaluation. A character consists of 1 start, 8 data, and 2 stop bits. Data rate is selectable from 300 to 19,200 baud.

Serial Data Structure: Response to a "T" command is:

(CR)(LF)I(SPACE)(SPACE)DDD(SPACE)HH:MM:SS(SPACE)(SPACE)TZ=XX(CR)(LF)

where:

I = space if clock set by WWVB (TIME SYNC lamp on)
    * if clock set manually via RS-232 port
    ? if time sync lamp is off
DDD = day of the year
HH:MM:SS = hours:minutes:seconds
XX = time zone switch setting at rear panel
Output is in UTC minus the time zone switch setting.

Option 30 Fully Decoded Text Stream: This alternate data format can be furnished when the unit is purchased:

(CR)(LF)I(SPACE)WWW(SPACE)DDMMMYY(SPACE)HH:MM:SS(CR)(LF)

where: I = as defined above
WWW =day of week (MON, TUE, WED, etc.)
DD = numeric day of month (01 to 31)
MMM = month (JAN, FEB, MAR, APR, etc.)
YY = year without century (83, 84, 85, etc.)
HH:MM:SS = as defined above.

"S" Command - to manually set the clock, enter:

SDDDHHMMSS

where: S = set command
DDD = UTC day of year
HH = UTC hours
MM = minutes
SS = seconds

Entry of the last seconds digit sets the clock to UTC time minus the time zone switch settings. The WWVB-derived on-time pulse increments the clock every second. If phase lock to the carrier has been acquired, the on-time second pulses are phase locked to the time code pulses even though the unit may temporarily be unable to decode the incoming signal. Thus, if the manual setting started the clock within one second after the correct on-time pulse, it will run truly on-time, as though it had set itself.

If Option 30 is present and the operator enters 366 for DDD day and the internal year switch is not set to a leap year, then the error message "*CHK YEAR SW" will be printed.

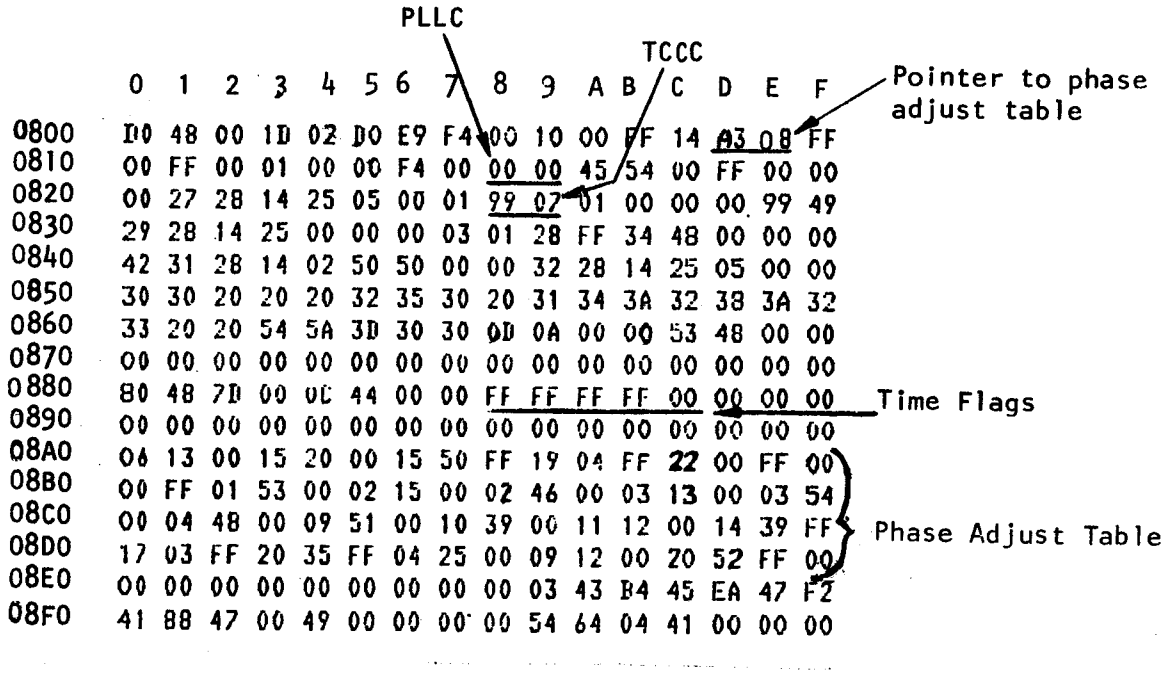
"D" Command - the "dump the memory" command, will print the contents of the 256-byte RAM memory. Performance event counters stored in RAM are:

Phase Lock Lost Counter PLLC
Time Code Compare Counter TCCC

The print out represents physical address locations 0800 through 08FF. The data is printed in hexadecimal notation. PLLC is a two-byte counter whose contents are printed at row 0810, columns 8 and 9. The first byte is the least significant byte. The counter records the number of times phase lock has been lost since power-on.

The Time Code Compare Counter, TCCC, records the number of times the received data compares with the expected value. It is printed at row 0820, columns 8 and 9. It is a 2-byte hexadecimal number printed least significant byte first.

Figure 1-4 is the print-out from a sample dump command.



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0800	D0	48	00	1D	02	D0	E9	F4	00	10	00	FF	14	A3	08	FF
0810	00	FF	00	01	00	00	F4	00	00	00	45	54	00	FF	00	00
0820	00	27	28	14	25	05	00	01	99	07	01	00	00	00	99	49
0830	29	28	14	25	00	00	00	03	01	28	FF	34	48	00	00	00
0840	42	31	28	14	02	50	50	00	00	32	28	14	25	05	00	00
0850	30	30	20	20	20	32	35	30	20	31	34	3A	32	38	3A	32
0860	33	20	20	54	5A	3D	30	30	0D	0A	00	00	53	48	00	00
0870	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0880	80	48	7D	00	0C	44	00	00	FF	FF	FF	FF	00	00	00	00
0890	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
08A0	06	13	00	15	20	00	15	50	FF	19	04	FF	22	00	FF	00
08B0	00	FF	01	53	00	02	15	00	02	46	00	03	13	00	03	54
08C0	00	04	48	00	09	51	00	10	39	00	11	12	00	14	39	FF
08D0	17	03	FF	20	35	FF	04	25	00	09	12	00	20	52	FF	00
08E0	00	00	00	00	00	00	00	00	00	00	03	43	B4	45	EA	47
08F0	41	88	47	00	49	00	00	00	00	54	64	04	41	00	00	00

FIGURE 1-4 SAMPLE MEMORY DUMP

1.3.5 PHASE ADJUST TABLE

The 1 PPS on-time pulse is phase locked to the leading edge of the received time code signal. After the initial turn-on sequence the phase adjustments are in 0.1 millisecond increments. Each time an adjustment is made the time and direction of the adjustment are logged in a circular table. The table is located at 08A0 through 08DE. The table contains the data on the last 21 phase adjustments. UTC hours and minutes followed by 00 or FF are logged, where 00 indicates the 1 PPS was shifted 0.1 millisecond left (early) and FF indicates that the 1 PPS was shifted 0.1 millisecond right (late). The current position pointer is located at row 0800, columns D and E, least significant byte first. This points to the memory location where the next adjustment will be stored.

After the unit has been on a few days the adjustment interval will exceed 24 hours. If adjustment data is desired the memory should be dumped at least once every 24 hours. This eliminates ambiguity concerning which day the adjustment was made.

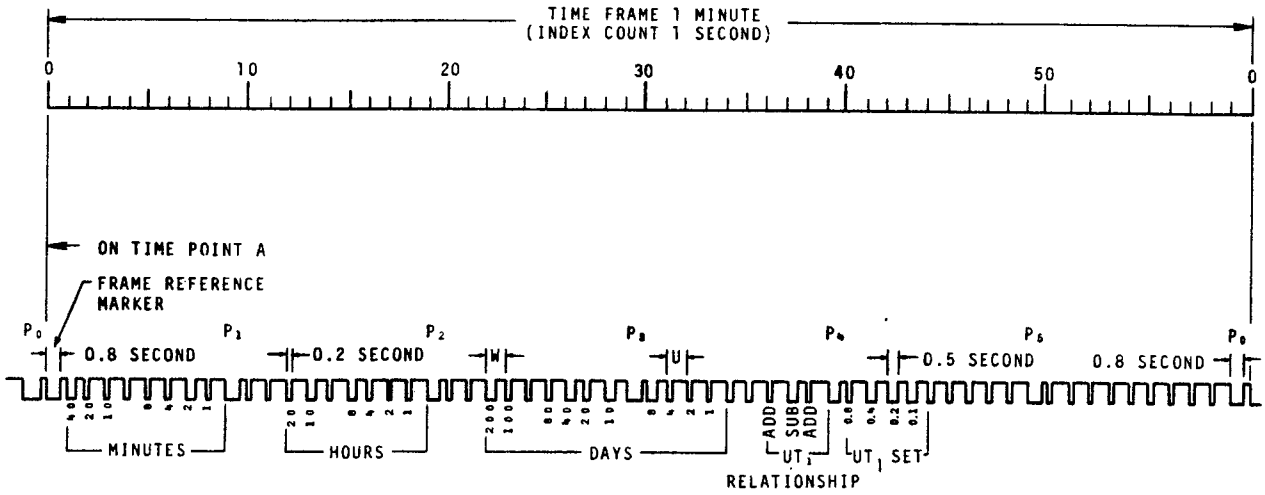
1.3.6 TIME FLAGS

At power-on or after the signal has been lost for longer than 180 minutes (depending on the setting of SW4-3,4) the Time Sync light will be off. This indicates that the time may be in error by greater than 100 milliseconds. The Time Sync light is turned on when a good time code is received. A received time code must pass a number of tests. When the seconds, minutes, hours and days portion of the time code are acceptable, flags are set to FF at row 0880, columns 8 through C. The clock is set and the Time Sync light is turned on when all the flags are set. This data is useful during the initial installation and trouble shooting to determine the progress of the self-setting process. When all the flags are set the TCCC is incremented, the flags cleared, and the process is repeated.

Once the Time Sync light is on the clock will keep UTC time. The display will be changed when 3 consecutive good compares are received that do not agree with the display data. This will happen when the leap second is inserted at the NBS WWVB transmitter.

1.3.7 TIME CODE FORMAT

The WWVB time code is generated at the transmitter by a 10-dB reduction of the carrier power of 10 dB at the beginning of each second. It is restored to a full power 200 milliseconds later for a binary zero, 500 milliseconds later for a binary one, and 800 milliseconds later for a position identifier. Decoding a one-minute data stream yields day of the year, time of day, and a correction factor for converting from atomic time (Coordinated Universal time, UTC) to earth time (UT1). Figure 1-5 WWVB TIME CODE FORMAT shows the coded data in a 1-minute time frame.



BINARY CODED DECIMAL TIME-OF-YEAR CODE WORD (23 DIGITS)
CONTROL FUNCTIONS (15 DIGITS) USED FOR UT_1 CORRECTIONS
6 PPM POSITION IDENTIFIER MARKERS AND PULSES (P_0 THRU P_5)
(REDUCED CARRIER 0.8 SECOND DURATION PLUS 0.2 SECOND DURATION PULSE)
W - WEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.5 SECOND - BINARY ONE)
U - UNWEIGHTED CODE DIGIT (CARRIER RESTORED IN 0.2 SECOND - BINARY ZERO)

NOTE: BEGINNING OF PULSE IS REPRESENTED BY NEGATIVE - GOING EDGE.

UTC AT POINT A	UT1 AT POINT A
258 DAYS	258 DAYS
18 HOURS	18 HOURS
42 MINUTES	41 MINUTES
	59.3 SECONDS

9/75

FIGURE 1-5 WWVB TIME CODE FORMAT

1.3.8 PROPAGATION PATH DELAY

Radio waves at low frequencies use the earth and the ionosphere as a waveguide and follow the earth's curvature for long distances. To compute the propagation path delay the great circle distance between the two points is divided by the speed of light.

The approximate formula for finding the great circle distance from Ft. Collins, Colorado, to another point in the northern hemisphere is given below. The error is 2% or less.

$$\text{Distance} = 60 \cos^{-1} (.758 \cos (\text{LAT}) \cos (\text{P}) + .652 \sin (\text{LAT}))$$

nautical miles.

where: LAT = latitude of receiver
P = (Longitude of WWVB) - (longitude of receiver)
WWVB is at 105°02' 39.5" W longitude
The speed of light is 300 Km/millisecond

To convert from nautical miles to millisecond delay:

$$\text{PATH DELAY} = \frac{\text{Nautical Miles} \times 1.8522 \text{ Km/Nautical mile}}{300 \text{ Km/msec}}$$

An example of the calculation is given below for Boston:

$$\text{PATH DELAY} = \frac{1521 \text{ nautical miles} \times 1.8522 \text{ Km/nautical mile}}{300 \text{ Km/msec}}$$

$$= 9.4 \text{ milliseconds}$$

The path delay from the WWVB transmitter in Ft. Collins, Colorado, to Boston is 9.4 milliseconds.

Figure 1-6 Path Delay Map shows the United States with concentric circles around Ft. Collins, Colorado. The radius of the inner circle is 600 Km and represents a 2 millisecond path delay. Outer circles represent increasing 2 millisecond delays. The map provides only an approximate value for path delay.

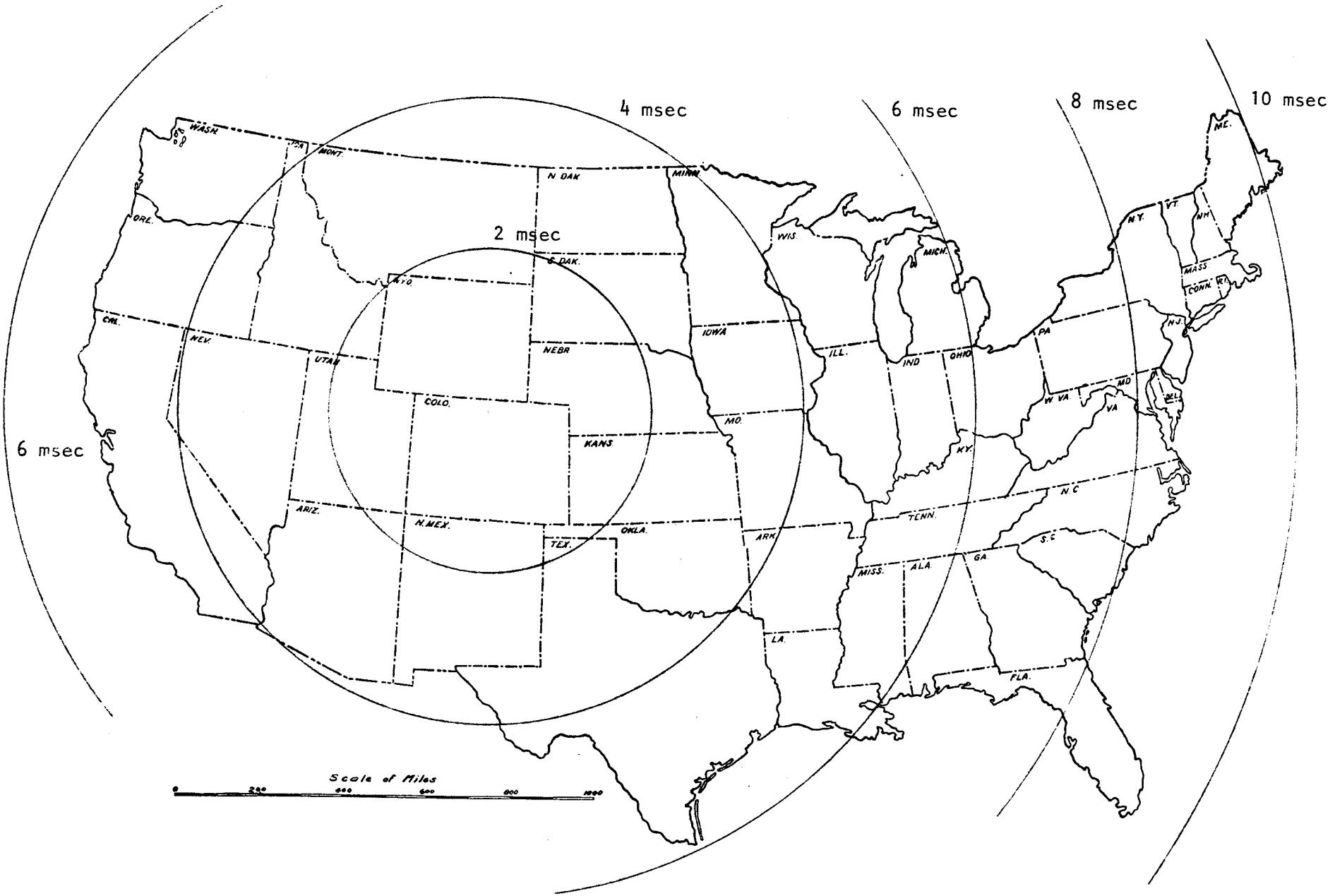


FIG. 1-6 PATH DELAY MAP

1.4 SPECIFICATIONS

1.4.1 MECHANICAL & INSTALLATION

Size: 3.5H x 13D x 17W (inches). Height is 4.25 inches including feet. If feet are removed, unit may be mounted in a 3 1/2" rack space.

88.9H x 330.2D x 431.8W (mm). Height is 107.9 mm including feet.

Handles protrude 1.75 inches (45mm) from front panel.

Allow 2-3 inches cable clearance at rear.

Weight: 13 lbs. (5.9 Kg): Shipping Wt. 16 lbs. (7.26 Kg).
Line Power: 115/230 VAC ±10%, 50/60 Hz, 0.2 Amps.
Operating Temperature: 0 to 50°C.

1.4.2 TIME ACCURACY

Ultimate Accuracy: ±0.1 msec

Overall Accuracy: ±(0.1 msec + noise uncertainty + propagation and receiver delay calibration error)

Noise Uncertainty: Less than ±0.5 msec when atomospheric signal-to-noise ratio is -10 dB in a 1.0 KHz bandwidth at the antenna (expected summertime worst case in U. S. coastal areas.)

Short-term jitter: 1.0-Hz on-time pulses are phase locked to the received time code and to the WWVB carrier and phase-corrected in 0.1-msec steps. The correction interval varies from about 1 hour to several days. The typical peak-to-peak jitter is less than 2 microseconds.

1.4.3 AUX IN/OUT

The AUX IN/OUT connector on the rear panel is the interface connector to the Model 8160A, 8161, or 8164. The connector is a 15-pin Molex connector (R03-09-1151.) Figure 1-7 shows the connector as viewed from the rear of the unit.

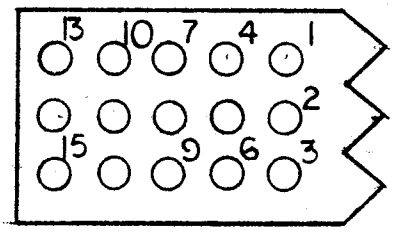


FIGURE 1-7 AUX IN/OUT CONNECTOR

Interface signals and pin assignments are listed below:

SIGNAL	PIN
10 MHz	13
10 MHz Shield	14
Phase Lock	5
Time Code	7
Time Code Shield/ Phase Lock Shield	4
Enable	9
Inhibit	12

The signal functions and specifications are:

10 MHz: Phase locked to the WWVB carrier, 3.4V rectangular pulse into 100 ohms. TTL-compatible.

Phase Lock: Indicates when receiver output is phase locked to the WWVB carrier. Ground level when unlocked, +5 VDC behind 3.3K ohms when locked.

Time Code: BCD time code yielding date and time of day. Logic high is +5 VDC behind 3.3K ohms, low is ground.

Enable: +5 Volts behind 100 ohms. Jumpered to INHIBIT signal in cable. Enables tri-state RS-422 driver.

Inhibit: Input impedance is 1000 ohms to ground. Connected to control input of RS-422 driver.

1.4.4 1 PPS ON-TIME OUTPUT

A positive-going signal phase locked to the leading edge of the WWVB 10-dB power reduction. The signal has a 10% duty factor and is TTL-compatible. BNC connector.

1.4.5 1-MHZ STANDBY INPUT

This signal is AC coupled into a 100-ohm terminating resistor. The signal level must be a minimum of 1 V peak-to-peak and a maximum of 10 V peak-to-peak. A BNC connector is used.

1.4.6 IRIG OUTPUT

If Option 23, IRIG B is present, then the Serial IRIG signal is brought out on this connector. The type of signal is selected internally by SW6.

SW6 ON TTL 50-ohm line driver output signal.

SW6 OFF A 1-KHz amplitude modulated sine wave. The open circuit output signal is nominally 8 volts peak-to-peak for a MARK and 2.4 volts peak-to-peak for a space. The output impedance is 50 ohms. It will drive a 600-ohm or greater load.

1.4.7 366/365 SWITCH

This leap year switch insures proper roll-over on day 366 and roll-back on day 1.

1.4.8 TIME ZONE SWITCH

This is a two-digit thumbwheel switch with a range of 00 to 19. The time displayed is UTC time received less the thumbwheel switch setting.

1.4.9 PATH DELAY SWITCH

This is a three-digit thumbwheel switch used to correct for propagation delay of the signal from Ft. Collins, Colorado, and receiver delay. Range is 00.0 to 99.9 milliseconds.

1.4.10 REMOTE OUTPUT CONNECTOR - OPTION 19

The Option 19 Remote Output Connector is a 9-pin series D receptacle (female). Figure 1-8 shows the pin locations viewed from the rear of the Model 8171. Option 19 is standard on units with serial numbers 8171-0566 and higher.

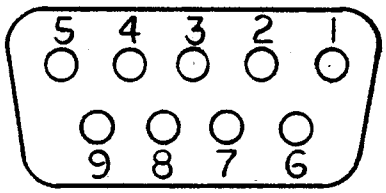


FIGURE 1-8 REMOTE CONNECTOR

SIGNAL	MNEMONIC	REMOTE CONNECTOR_PIN	SERIAL ASCII CONNECTOR_PIN
BUS DATA	-BDATA	J11-3	
BUS DATA	+BDATA	-8	
BUS ON-TIME	-BON-TIME	J11-2	
BUS ON-TIME	+BON-TIME	-7	
BUS TIME SYNC	-BTSYNC	J11-1	
BUS TIME SYNC	+BTSYNC	-6	
ENABLE	ENABLE	J11-4	
GROUND	GND	-9	
TIME DATA	TDATA	J11-5	J11-19

BDATA, BON-TIME and BTSYNC signals conform to EIA RS-422 standard. TDATA conforms to RS-232C signal levels.

The +BON-TIME signal is a positive-going 0.1-second pulse relative to -BON-TIME, occuring once per second. The leading edge of the pulse is the beginning of the second.

The +BTSYNC signal is high relative to -BTSYNC after the NBS time code has been decoded. The signal goes low n minutes after the receiver has lost phase lock with the NBS signal. The number of minutes, n, that the signal stays active after the receiver has lost phase lock is selected by switch A1A2 SW4-3,4. It remains low until another successful decoding is accomplished.

The ENABLE signal is +5 volts in series with 60 ohms.

1.4.11 SERIAL ASCII

The Serial ASCII port provides the day and time data in ASCII format. The interface is RS-232 compatible. The connector is a 25-pin series D female connector. The signal and pin numbers are listed below.

SIGNAL	MNEMONIC	PIN	
Protective Ground	AA	J4-1	
Transmit Data	BA	J4-2	(IN TO 8171)
Receive Data	BB	J4-3	(OUT OF 8171)
Clear-to-send	CB	J4-5	
Data Set Ready	CC	J4-6	
Signal Ground	AB	J4-7	
Received Line Signal Detector	CF	J4-8	

The Clear-to-Send signal is connected to +12 VDC through a 5.6K resistor. The Received Line Signal Detector and Data Set Ready will be high when power is on, and are connected together and tied to +12 volts through a 5.6K resistor.

The time data is sent out in response to a "T" command. The data represents the time at the beginning of the first character sent. The bit rate is selectable by switch A1A2 SW2. Refer to Section 1.2.8 Internal Switches for information on bit rate selection.

Relative to RS-232 definitions, the Model 8171 is a data communication equipment DCE. Transmit Data, BA, is to the Model 8171. Received Data, BB, is from the Model 8171.

1.4.12 BUS B

BUS B is an RS-422 bus. The connector is a 14-pin plug, AMP CHAMP part 552739-1 or equivalent. The signals and pin assignments are listed below:

SIGNAL	MNEMONIC	PIN
+1 MHZ	Y1MHZ	5
-1 MHZ	Z1MHZ	12
+ØLOCK	YØLK	2
-ØLOCK	ZØLK	9
+TCODE	YTCD	6
-TCODE	ZTCD	13
GND	GND	1
GND	GND	8

Pin reference numbers are on the connector.

1.4.13 BUS A

BUS A is an extension of BUS B. The BUS B signals appear on corresponding pins on BUS A. The connector is a 14-pin receptacle, AMP CHAMP part 552738-1 or equivalent.

1.4.14 PARALLEL BCD - OPTION 18

The Parallel BCD Output option provides day and time data in Parallel BCD format on a 50-pin connector. All lines are TTL-compatible.

Data is valid from 20 milliseconds before the ON-TIME pulse until 850 milliseconds after the ON-TIME pulse. Signals are positive logic, i.e. a logical 1 is high, a logical 0 is low.

There will be no data out until the clock has been set by WWVB or by the manual SET command.

1.4.15 TIME SYNC - FRONT PANEL LED

The green lamp is turned on when the time code is fully decoded. In order to select the length of time before the time sync lamp goes out after loss of phase lock, switch (SW4-3,4) can be set to select 1 of 4 times:

SW4-4 Setting	SW4-3 Setting	Time (min)	Typical Error (msec)
0	0	10	1
0	1	20	10
1	0	60	30
1	1	180	100

The lamp will come back on after the receiver reacquires phase lock to the WWVB carrier and the time code is decoded.

1.4.16 STAND-BY CRYSTAL OSCILLATOR

Temperature Stability 20°C to 30°C: $\pm 1 \times 10^{-6}/°C$
Aging Rate: 2×10^{-6} for first 6 months, 2×10^{-6}/year thereafter.
Frequency Adjustment: Sufficient to compensate for 10 years of aging.
Adjustment Resolution, 1×10^{-7}
Accuracy: Set at the factory to $\pm 1 \times 10^{-6}$

1.4.17 SELECTABLE BIT RATE

The Serial ASCII output is internally switch-selectable to 75, 150, 300, 600, 1200, 2400, 9600, 19,200, and 110 bits per second by switch A2A1 SW2 located in position marked U11. Refer to Section 1.2.8 for bit rate select table.

1.4.18 OPTIONS IN NUMERICAL ORDER

Option 01: Rack Mount Kit
Option 11: Rack Mount with Slides
Option 18: Parallel BCD
Option 19: Remote Output Driver (standard on all units with serial numbers 8171-0566 and higher)
Option 23: IRIG B Output
Option 24: TCXO (Temperature Controlled Crystal Oscillator)
Option 30: Fully Decoded Text Stream

SECTION 2

8171A

THEORY OF OPERATION

2.1 Introduction

2.2 Microprocessor Assembly

2.3 Display Assembly

2.4 DC Power Supply Assembly

2.1 INTRODUCTION

The 8171A Synchronized Clock consists of a Microprocessor Assembly, a Display Assembly, and a Power Supply Assembly, as shown in Figure 2-1 Block Diagram, Microprocessor Assembly.

The phase-locked 10 MHz, phase lock condition signal, and detected time code outputs of the Model 8160A, 8161, or 8164 Receiver are fed into the input of the microprocessor. In addition to the front panel display, day and time data are supplied in ASCII format via the RS-232 interface on the rear panel.

The Microprocessor Assembly consists of an 8085A microprocessor, 6K of EPROM, 512 bytes of RAM, 2 timer chips, a priority interrupt controller, a USART, RS-422 receivers and transmitters, and an LED display interface.

The processor integrates out the noise, measures the time code pulse widths, decodes the signal, phase locks a 1-Hz on-time pulse to the WWVB input signal, and controls the display and time-of-year outputs.

Input signals from the thumbwheel switch on the rear panel provide time zone and path delay corrections.

2.2 MICROPROCESSOR ASSEMBLY, A1A2, P/N 015500

The Microprocessor Assembly decodes the WWVB time code signal output of the Receiver/Frequency Standard and compensates for propagation and receiver delays and for time zone differences. The time of day is displayed on the front panel. The day and time data are provided to the ASCII interface on the rear panel. An optional parallel BCD output of this information is also available.

Schematics of the Microprocessor Assembly are shown in Figure 2-2, sheet 1 through 8. The Layout is shown in Figure 2-3.

References to integrated circuits identify the sheet the circuit appears on, the physical location on the board and the pin number if one is referenced. For example, 4U14B-6 refers to an IC on sheet 4, physical location U14 on the board and pin 6.

The 10-MHz output of the Model 8160A/8161/8164 Receiver is fed to the input of the first Synchronized Clock in the chain to Line Receiver 4U27A, and then is divided by 10, in Divider 4U26, to provide 1 MHz to Line Transmitter 4U37. The output of 4U37 goes to J3 for connection to the input of the next Synchronized Clock in the chain, and also to Line Receiver 4U36. Synchronized Clocks other than the first one in the chain obtain the 1 MHz signal from the previous unit through J2 to the above Line Receiver input.

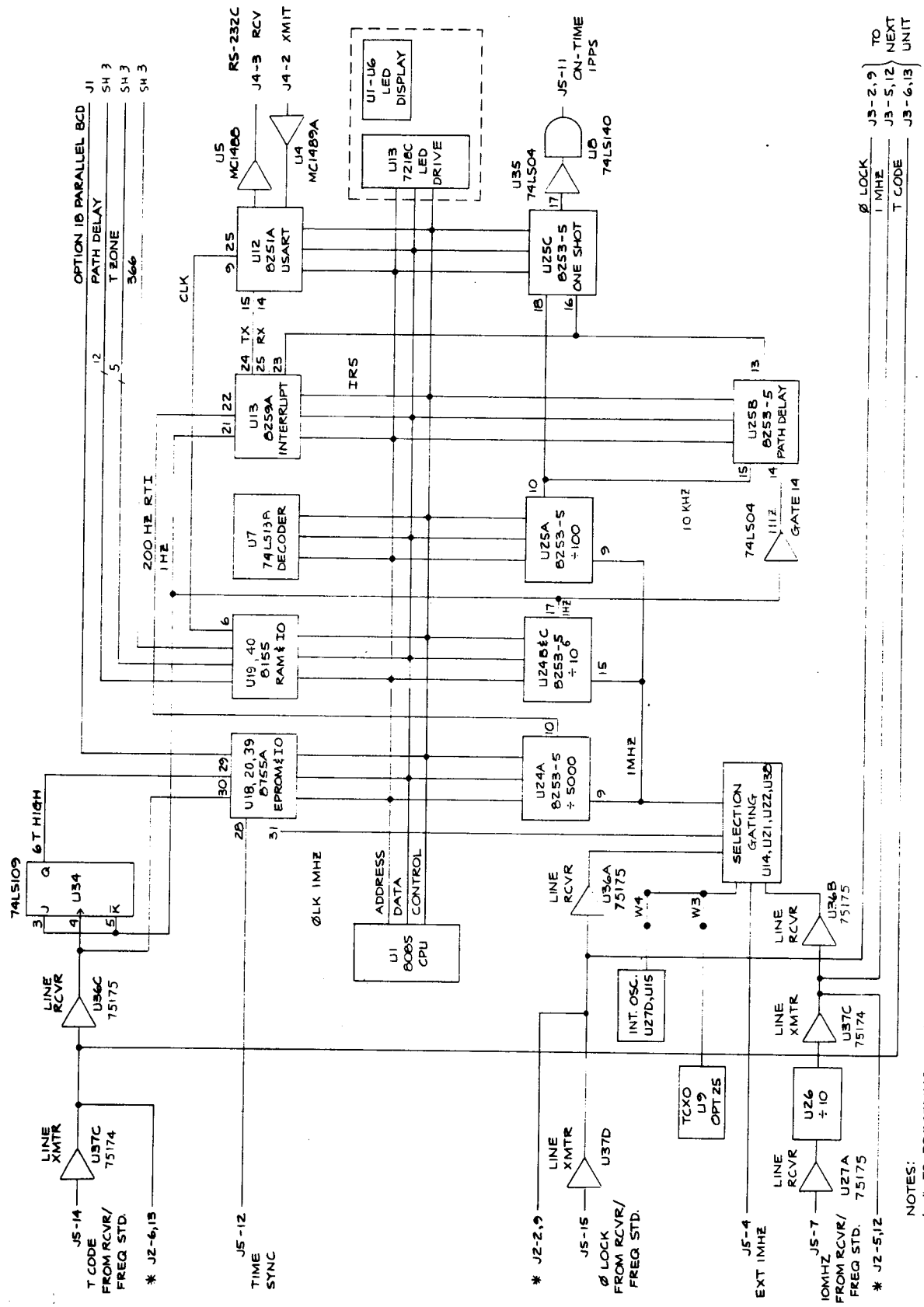


FIG. 2-1 MICROPROCESSOR BLOCK DIAGRAM

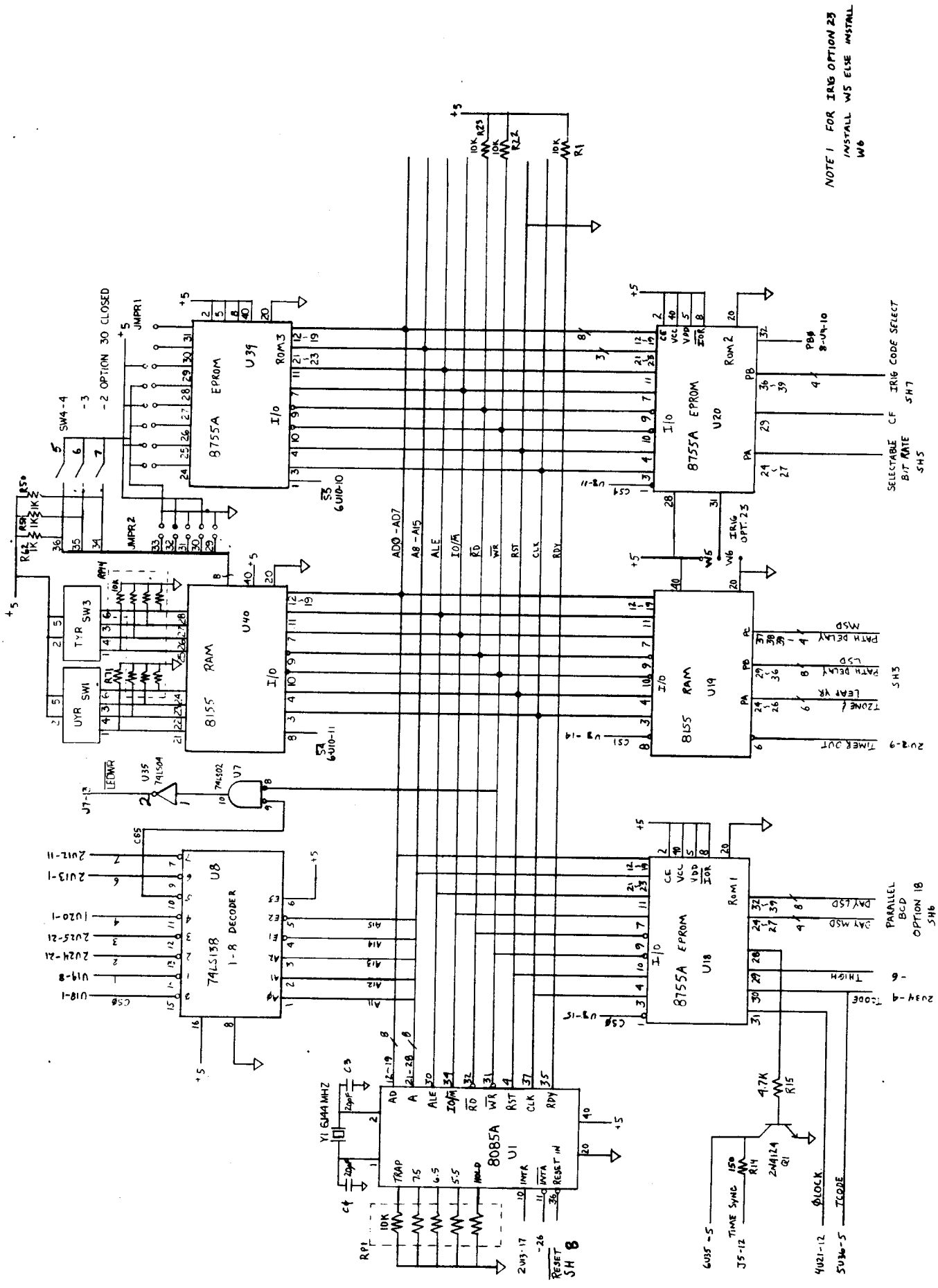
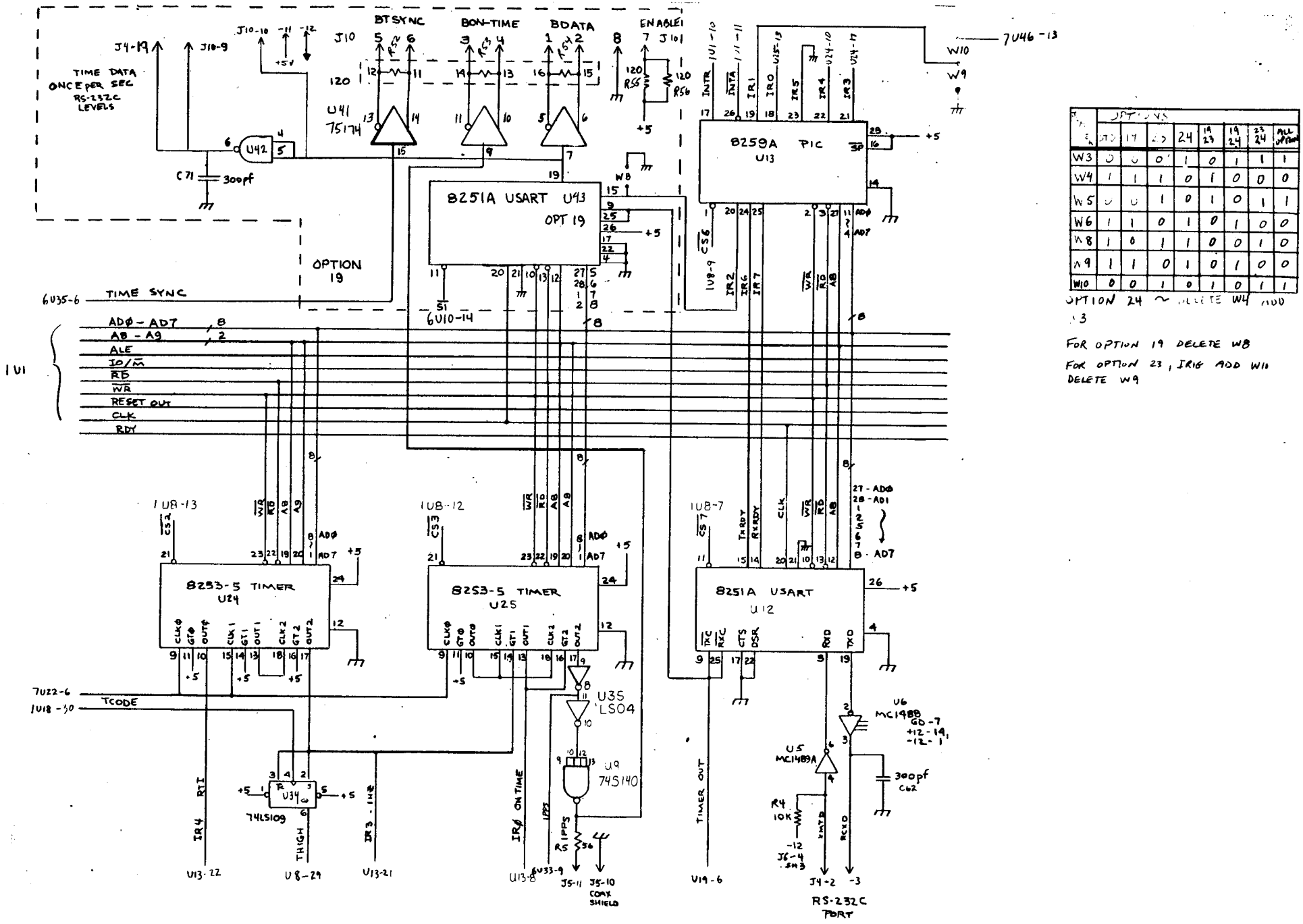


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 1



	OPTIONS							
	19	19	23	24	19 23	19 24	23 24	ALL OPTIONS
W3	0	0	0	1	0	1	1	1
W4	1	1	1	0	1	0	0	0
W5	0	0	1	0	1	0	1	1
W6	1	1	0	1	0	1	0	0
W8	1	0	1	1	0	0	1	0
W9	1	1	0	1	0	1	0	0
W10	0	0	1	0	1	0	1	1

OPTION 24 ~ DELETE W4 AND W3

FOR OPTION 19 DELETE W8

FOR OPTION 23, IRIG ADD W10 DELETE W9

FIGURE 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 2

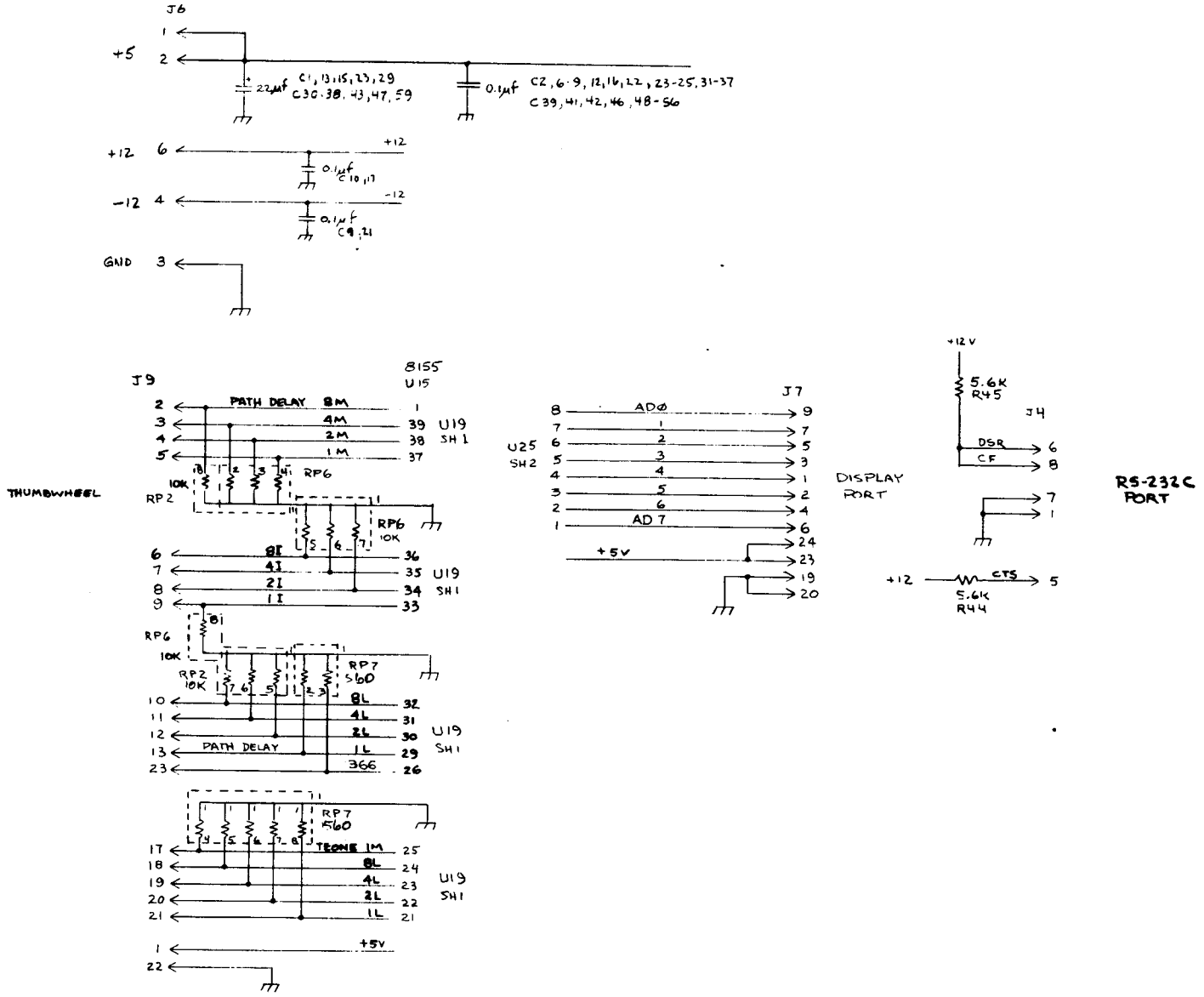


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 3

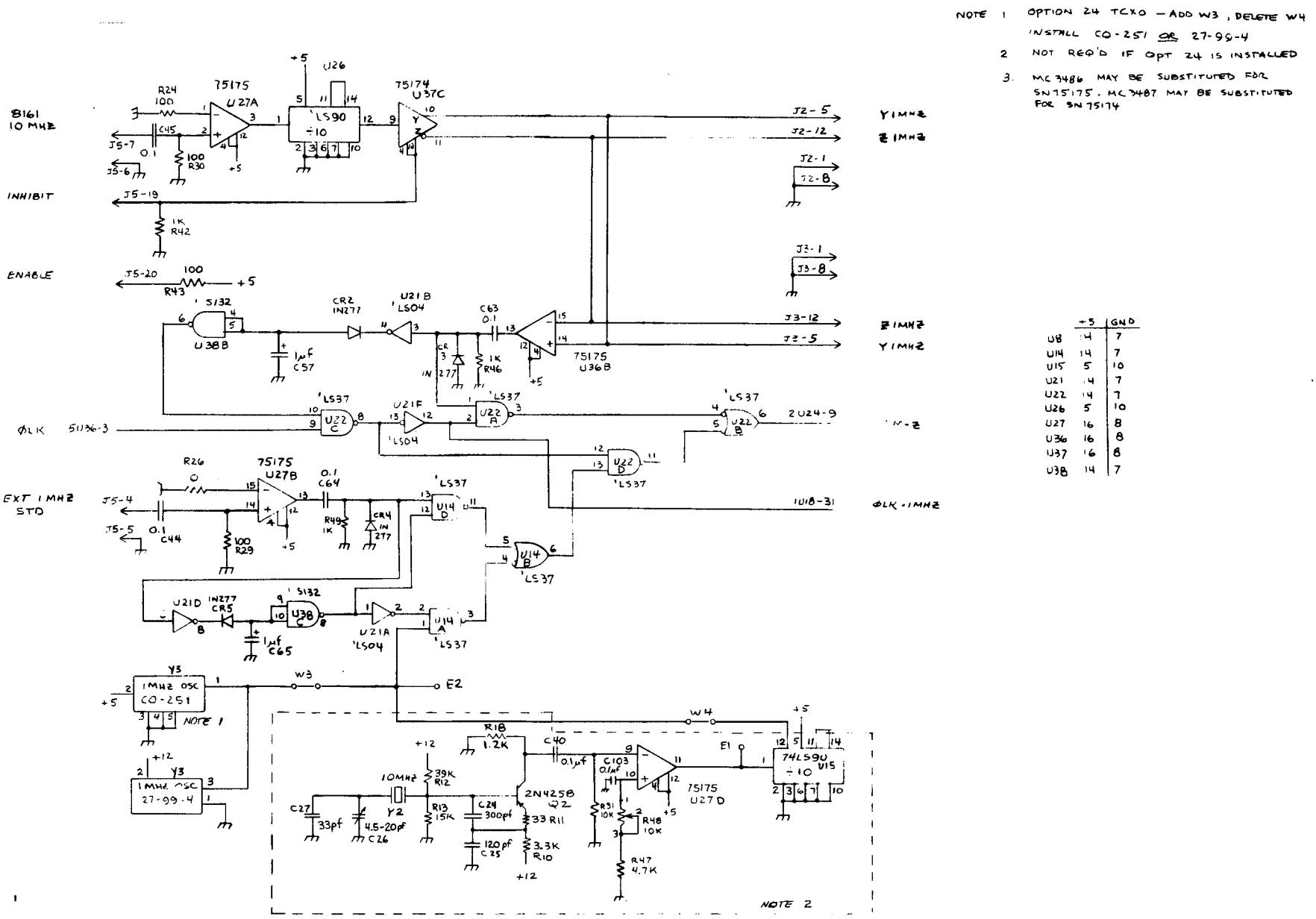


FIGURE 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 4

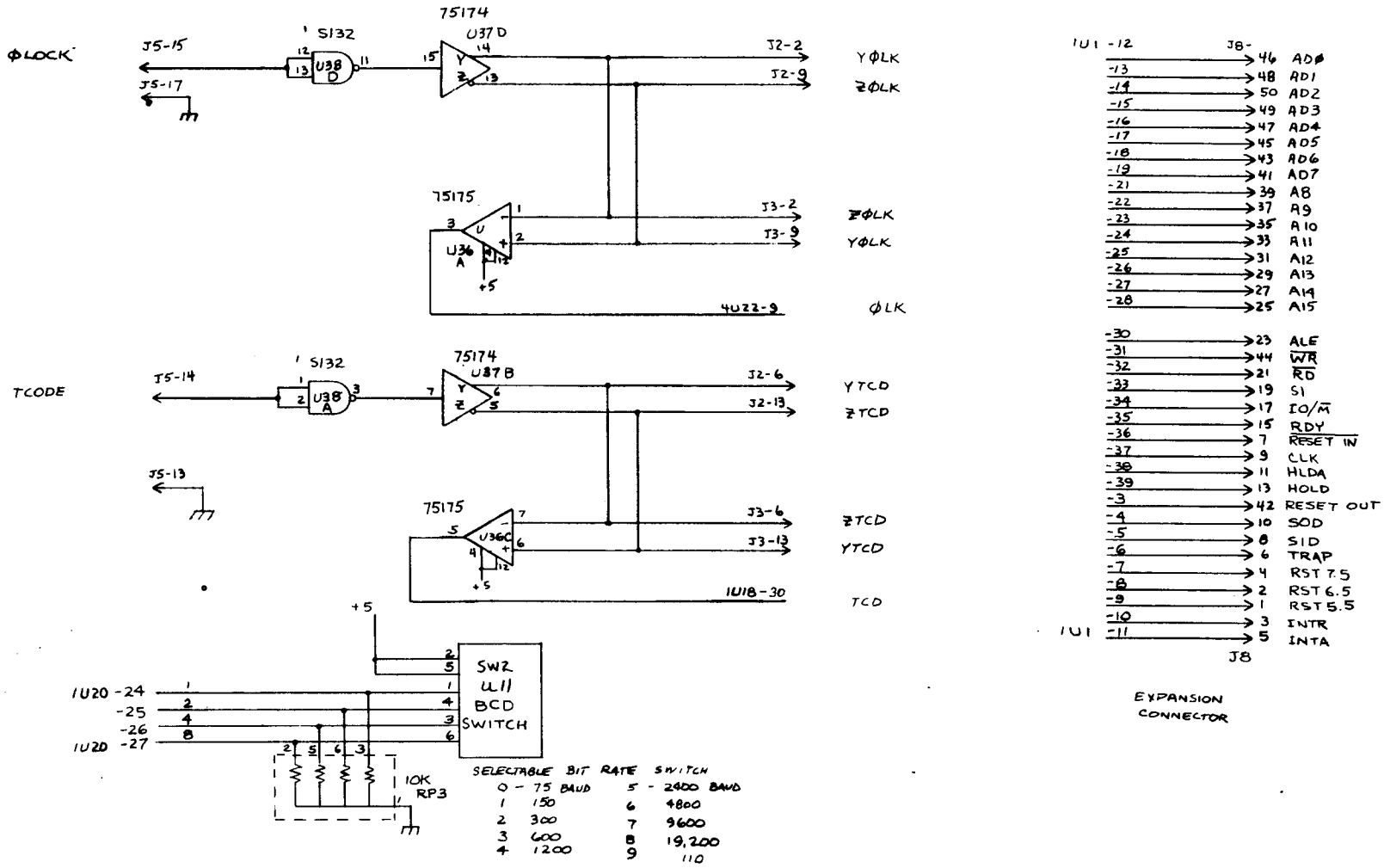
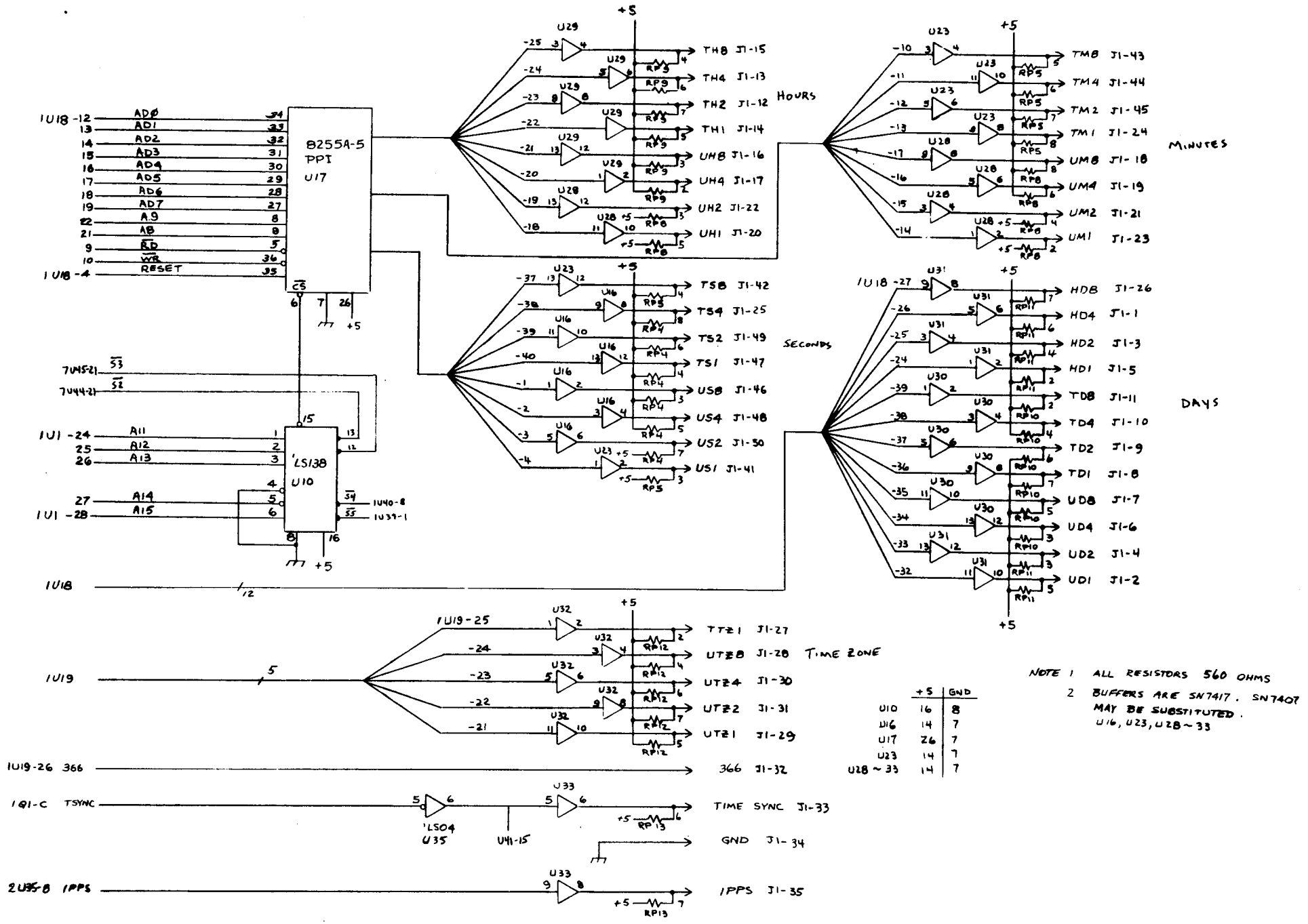
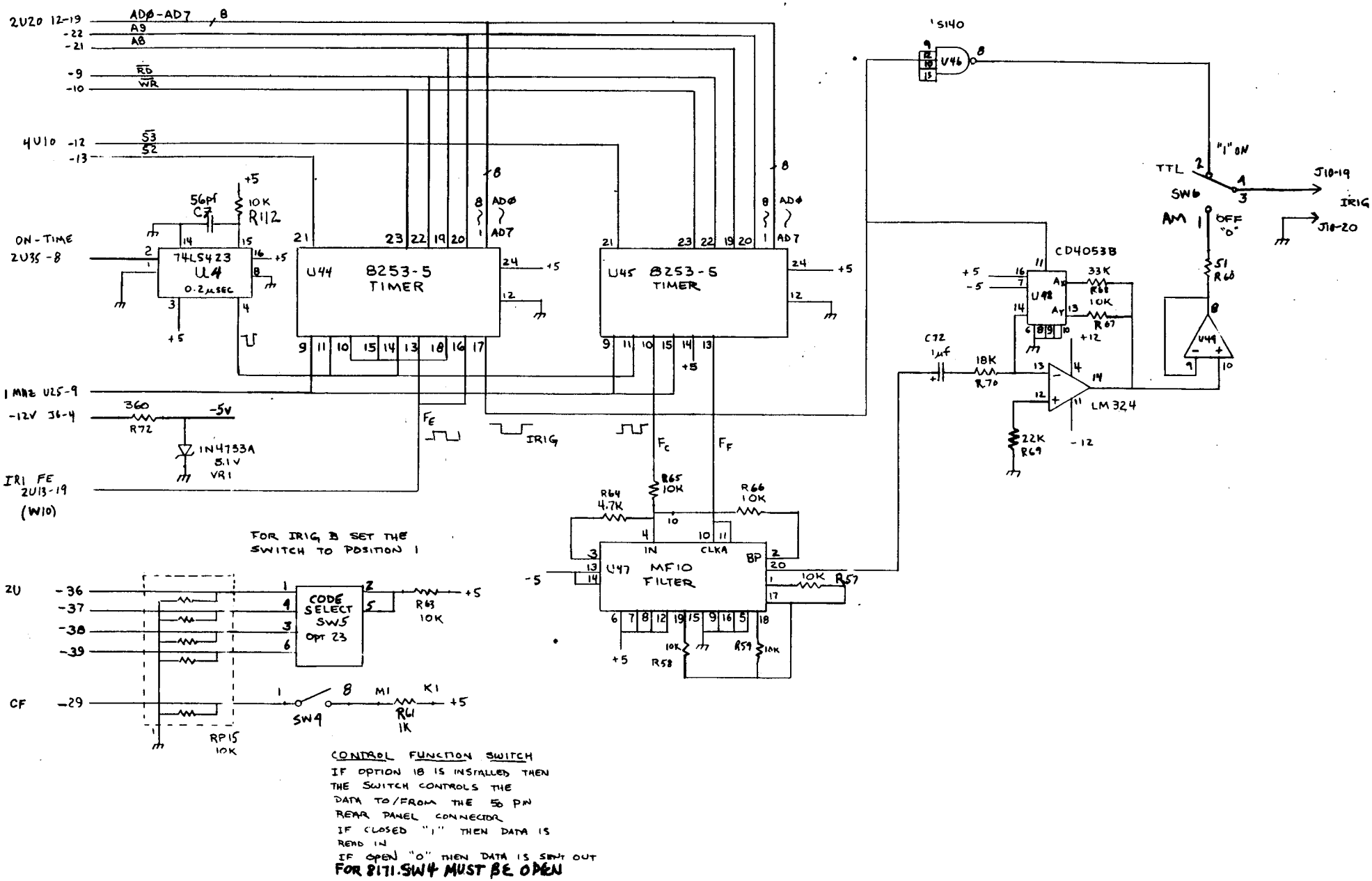


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 5



	+5	GND
U10	16	8
U16	14	7
U17	26	7
U23	14	7
U28 ~ 33	14	7

FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 6



CONTROL FUNCTION SWITCH
IF OPTION 18 IS INSTALLED THEN THE SWITCH CONTROLS THE DATA TO/FROM THE 50 PIN REAR PANEL CONNECTOR
IF CLOSED "1" THEN DATA IS READ IN
IF OPEN "0" THEN DATA IS SENT OUT
FOR 8171.SW4 MUST BE OPEN

FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 7

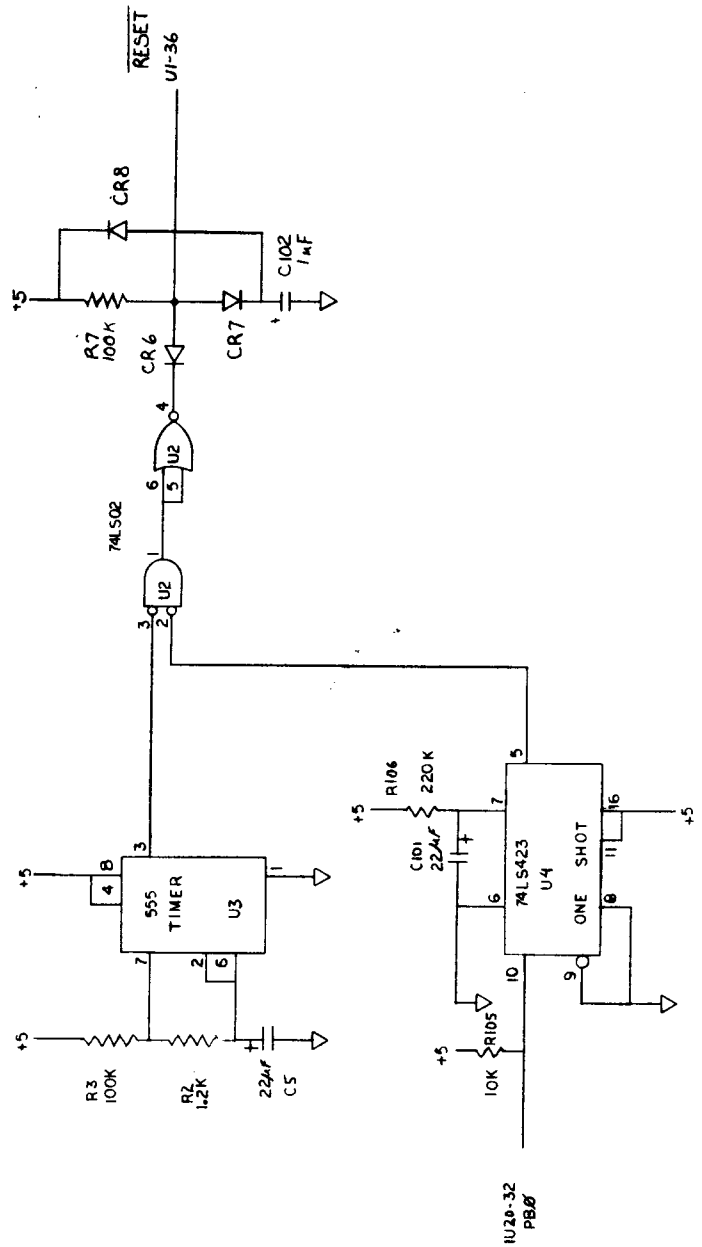


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 8

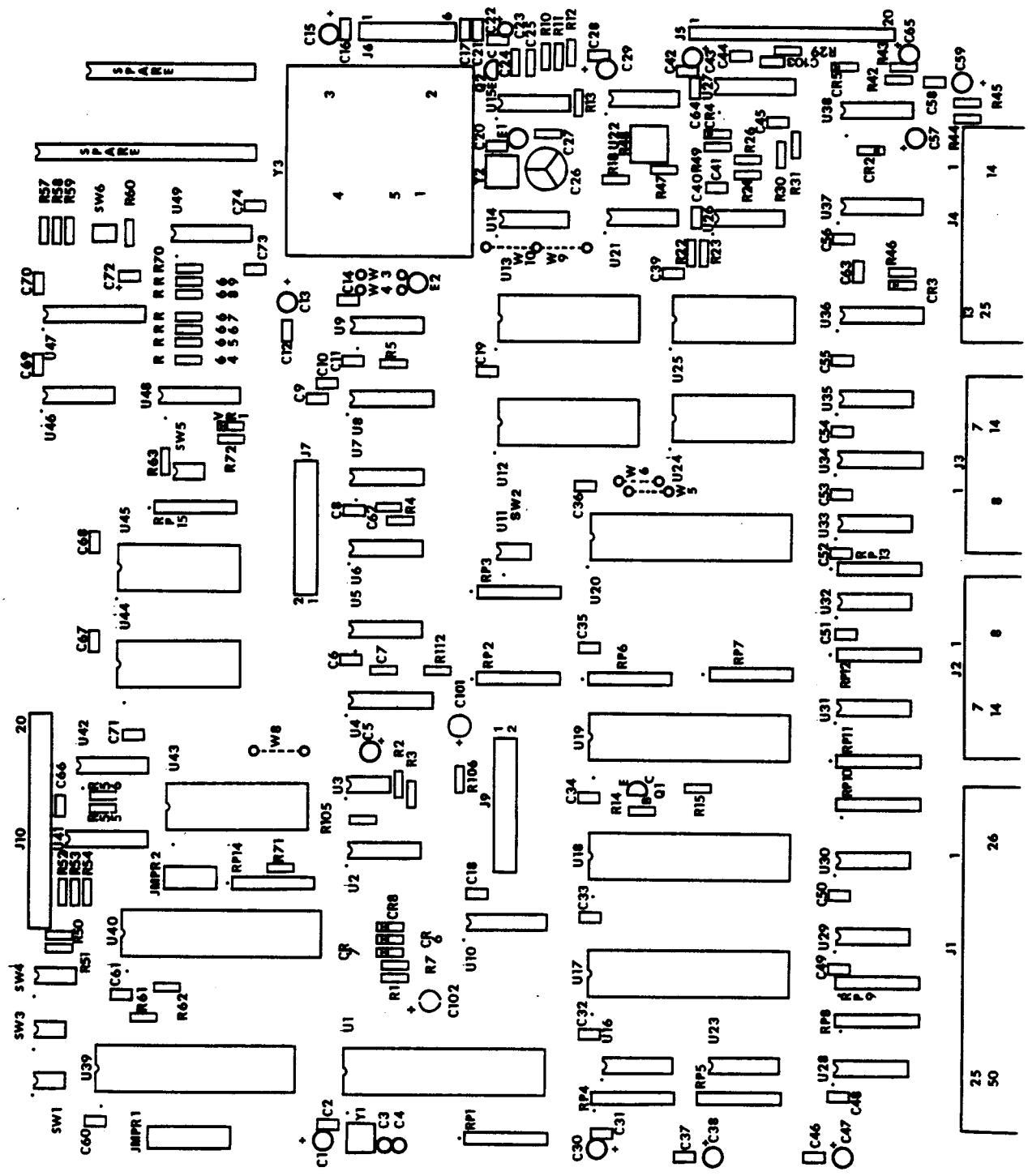


FIGURE 2-3 ASSEMBLY DRAWING - MICROPROCESSOR

The 1-MHz output of 4U36 is applied to a DC restorer consisting of C63, R46, and CR3. A level detector consisting of 4U21, CR2, and C57 at the output of the DC restorer provides a positive level at the output of 4U38B in the presence of the phase locked 1-MHz signal. This signal is gated with the phase lock status signal output of the Receiver at 4U22C. If both signals are present, a ground level appears at the output of 4U22C which is inverted through 4U21F to provide the (ØLK) (1-MHz) signal to EPROM 1U18.

The 4U21F output also enables the phase locked 1-MHz signal through 4U22A.

If either the phase locked 1-MHz signal or the phase lock status signal are not present, the output of 4U22C is positive, inhibiting any signal through 4U22A and enabling 4U22D. The other input of 4U22D will be the output of one of three backup oscillators.

The three backup oscillators are an external 1-MHz standard, a temperature-compensated crystal oscillator, TCXO, (Option 24) or an uncompensated crystal oscillator.

If a 1-MHz external oscillator is used, its output will be connected through Line Receiver 4U27B. A DC restorer consisting of C64, R49, and CR4 and a level detector consisting of 4U21, CR5, and C65 operate in the same manner as the circuits described above to enable gate 4U14D and to disable gate 4U14A.

When the external signal is not present, the DC restorer and level detector inhibit gate 4U14D and enable 4U14A allowing the internal oscillator or output to be applied to OR Gate 4U14B. The output of 4U14B is gated through 4U22D. OR Gate 4U22B allows the proper 1-MHz signal to be applied to Timer 2U24. Selection of the internal oscillator or the TCXO option is performed by internal jumpers W3 and W4.

The Phase Lock Status and Time Code signals from the Receiver are each brought in to the first Synchronized Clock in the chain on connector J5 to Schmitt trigger 5U38 and then to Line Transmitter 5U37, for connection through J3 to the next unit in the chain, and also through Line Receiver 5U36 to Gate 4U22C for the Phase Lock Status signal and to EPROM 1U18 for the Time Code signal. The inputs to Synchronized Clocks other than the first in the chain are derived from the previous Synchronized Clock through connector J2 to the input of 5U36.

The 10-MHz NBS phase locked signal is fed into Line Receiver 4U27 and then to 4U26 where it is divided by 10 to 1 MHz. This signal is divided by 5000 by 2U24A to provide a 200-Hz real-time interrupt, and it is divided by 1,000,000 by 2U24B and 2U24C to provide the 1-Hz on-time reference. It is divided by 100 by 2U25A to provide a 10-KHz signal which is fed as a clock input to path delay timer 2U25B. The path delay timer is gated on by the 1-Hz reference. An output pulse

will occur after a delay proportional to the setting of the path delay thumbwheel switch on the rear panel. The signal is fed into 2U25C, which is a programmable one-shot. The output is a 100-millisecond pulse whose leading edge is "on-time".

The time code, TCODE, signal is fed to Line Receiver 5U36 to input pin 30 on the 8755A EPROM 1U18 and to the clock input of a 74LS109 J-K flip-flop. The TCODE is sampled at a 5-millisecond rate by the microprocessor. Pulse widths are measured and decoded and the 1-Hz reference signal is phase locked to the leading edge of the time code.

The phase lock algorithm has two modes, fast sync and fine sync. In the fast sync mode, the 1-Hz reference is adjusted in 0.1-second steps until phase lock is achieved. The adjustment steps are progressively reduced to 1 millisecond. After the clock is set the steps are reduced to 0.1 millisecond. The time between adjustments is made progressively longer and will extend beyond 24 hours. Each time an adjustment is made the time and direction of the adjustment is logged in the Phase Adjust Table (See Section 1.3.5).

A serial RS-232 interface is provided by 8251A USART, 2U12. The XMTD input is received through Level Converter 2U5 and the RCXD output is sent through Level Converter 2U6. The DSR, CR, and CTS signals are connected through 5.6K ohms to +12 volts.

The processor runs under interrupt, with priorities controlled by the 8259A Programmable Interrupt Controller, PIC, 2U13.

The interrupt levels are:

IR0 - On-time pulse
IR1 - IRIG Frame Element (Option 23)
IR2 - Remote Output USART Xmit (Option 19)
IR3 - 1 Hz reference
IR4 - 200 Hz RTI
IR5 - On-time pulse
IR6 - USART Xmit
IR7 - USART Rcv

Chip selection is made by the LS138 1-8 Decoder, 1U8 and 6U10. The chip selects are:

CS0 -	1U18-1	8755A	EPROM & I/O
CS1 -	1U19-8	8155	RAM & I/O
CS2 -	2U24-21	8253-5	TIMER
CS3 -	2U25-21	8253-5	TIMER
CS4 -	1U20-1	8755A	EPROM & I/O
CS5 -	1U7-8	74LS02	LED DISPLAY
CS6 -	2U13-1	8259A	PROGRAMMABLE INTERRUPT CONTROLLER
CS7 -	2U12-11	8251A	USART

S0	- 6U17-6	8255A-5	PROGRAMMABLE PERIPHERAL INTERFACE (PPI) (Option 18)
S1	- 2U43-11	8251A	USART (Option 19)
S2	- 7U44-21	8253-5	TIMER (Option 23)
S3	- 7U45-21	8253-5	TIMER (Optio 23)
S4	- 1U440-8	8155	RAM & I/O
S5	- 1U39-1	8755A	EPROM & I/O (Option 23)

The Central Processing Unit (CPU) 1U1 is an 8085A with a 6.14-MHz crystal. Power-on reset is provided on pin 36 from the brown-out reset circuitry on sheet 8. Signals RD, WR and RDY are tied to +5 volts through Resistors R1, R22 and R23.

The On-time 1 PPS output is derived from the Timer, 2U25 via Driver 2U9. Data from EPROM 1U18 is decoded and latched in PPI 6U17 to provide the parallel BCD output (Option 18) through output drivers 6U16, 6U23, and 6U28 through 6U33.

A BCD switch, 5U11, is the data input for implementation of Selectable Bit Rate.

2.3 DISPLAY ASSEMBLY, A2A1, P/N 014100

The Display Assembly provides digital panel readout of time of day. Prior to receiving the phase lock signal from the Receiver, time since turn-on is displayed.

The layout of the Display Assembly is shown in Figure 2-4. The schematic is shown in Figure 2-5.

The display assembly is mounted on the rear of the front panel. It consists of ICM7218C LED Driver and six seven-segment LED digits that provide a 24-hour clock display.

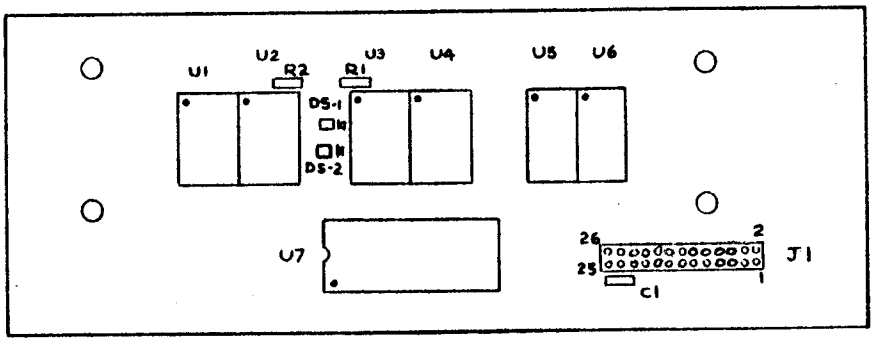


FIG. 2-4 ASSEMBLY DRAWING - DISPLAY ASSEMBLY

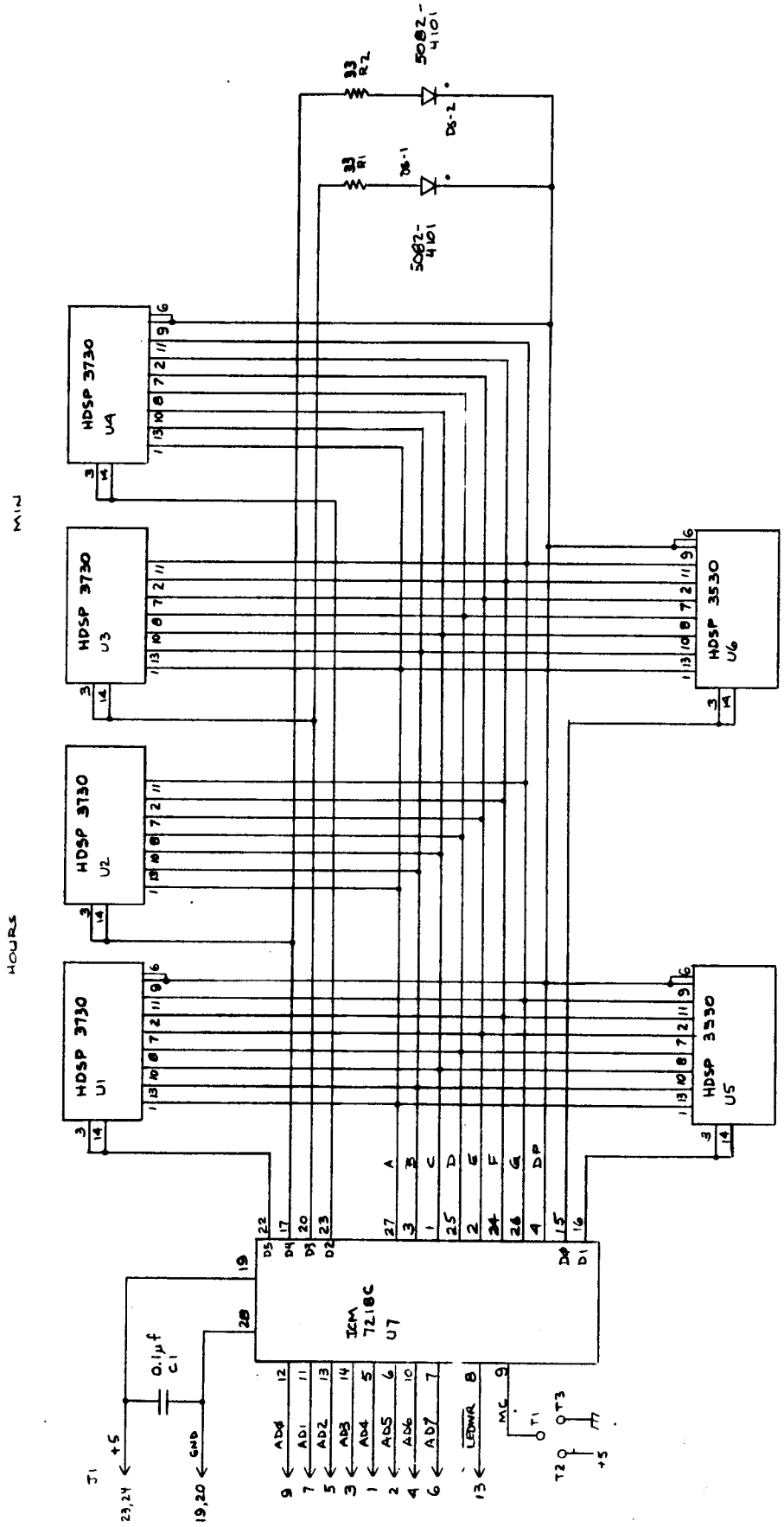


FIG. 2-5 SCHEMATIC, DISPLAY ASSEMBLY

2.4 DC POWER SUPPLY ASSEMBLY, A1A1, P/N 015300

The DC Power Supply Assembly provides +5 VDC, and ±12 volts DC for operation of the Microprocessor and Display Assemblies.

The layout of the DC Power Supply Assembly is shown in Figure 2-6. The schematic is shown is Figure 2-7.

The AC input for the DC power supplies is filtered by capacitors A1C1 and A1C2, then fed through Fuse F1 to transformer A1T1.

The +5 volt DC supply consists of full wave rectifiers, diodes CR1 and CR2, filter capacitors C1 through C7, regulator U1 and Zener diode VR1.

The +12 volt DC supply consists of a bridge rectifier, diodes CR3 through CR6, +12 volt regulator U2, -12 volt regulator U3, and filter capacitors C8 through C15.

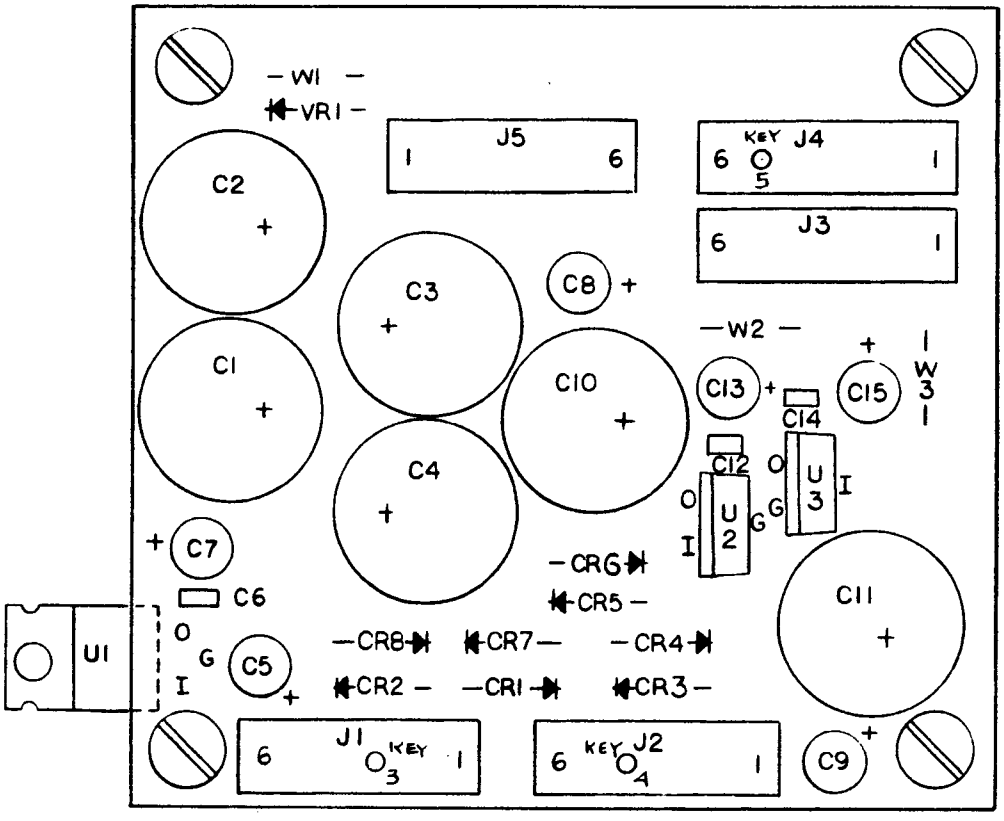


FIG. 2-6 ASSEMBLY DRAWING - DC POWER SUPPLY

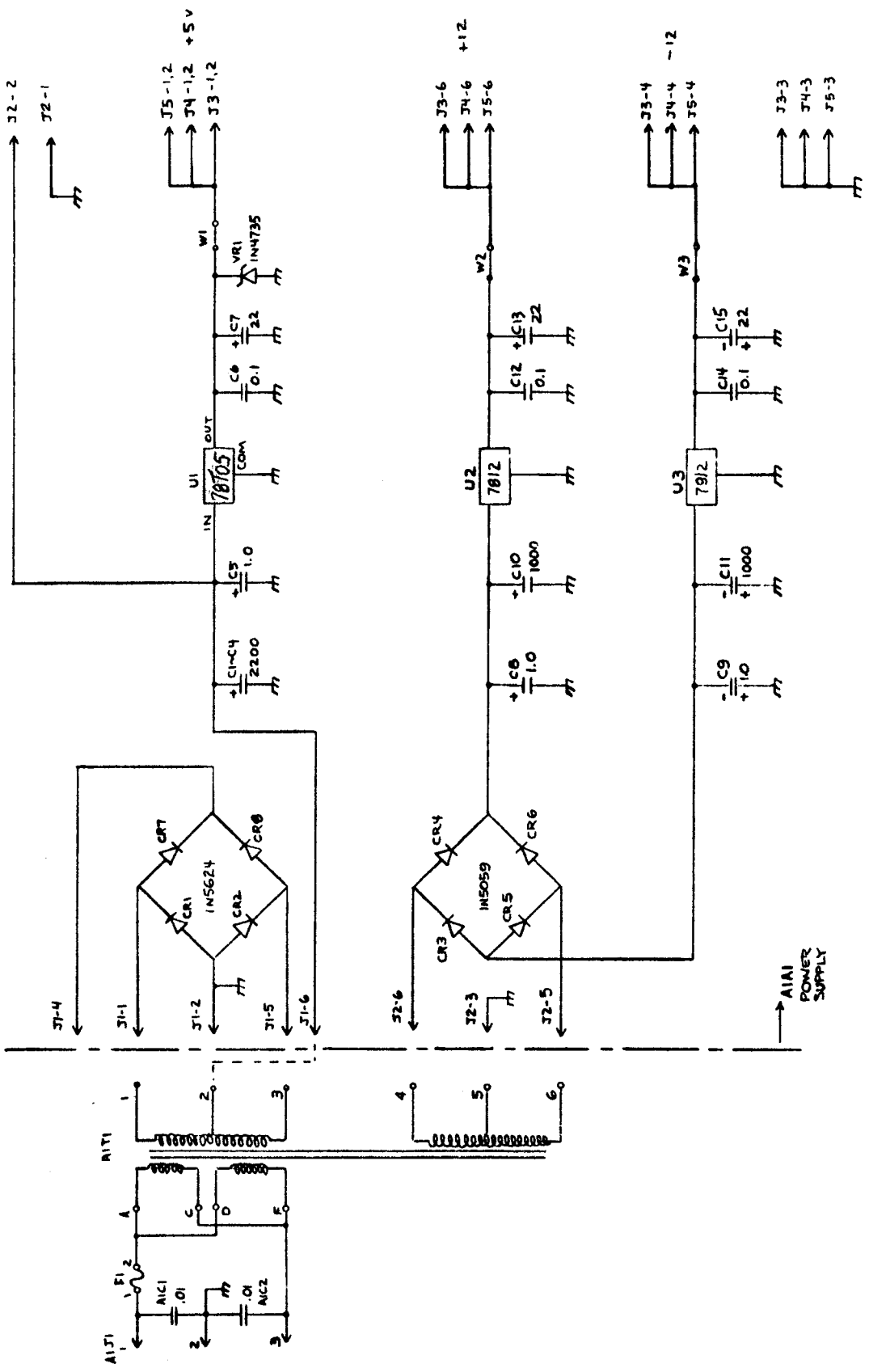
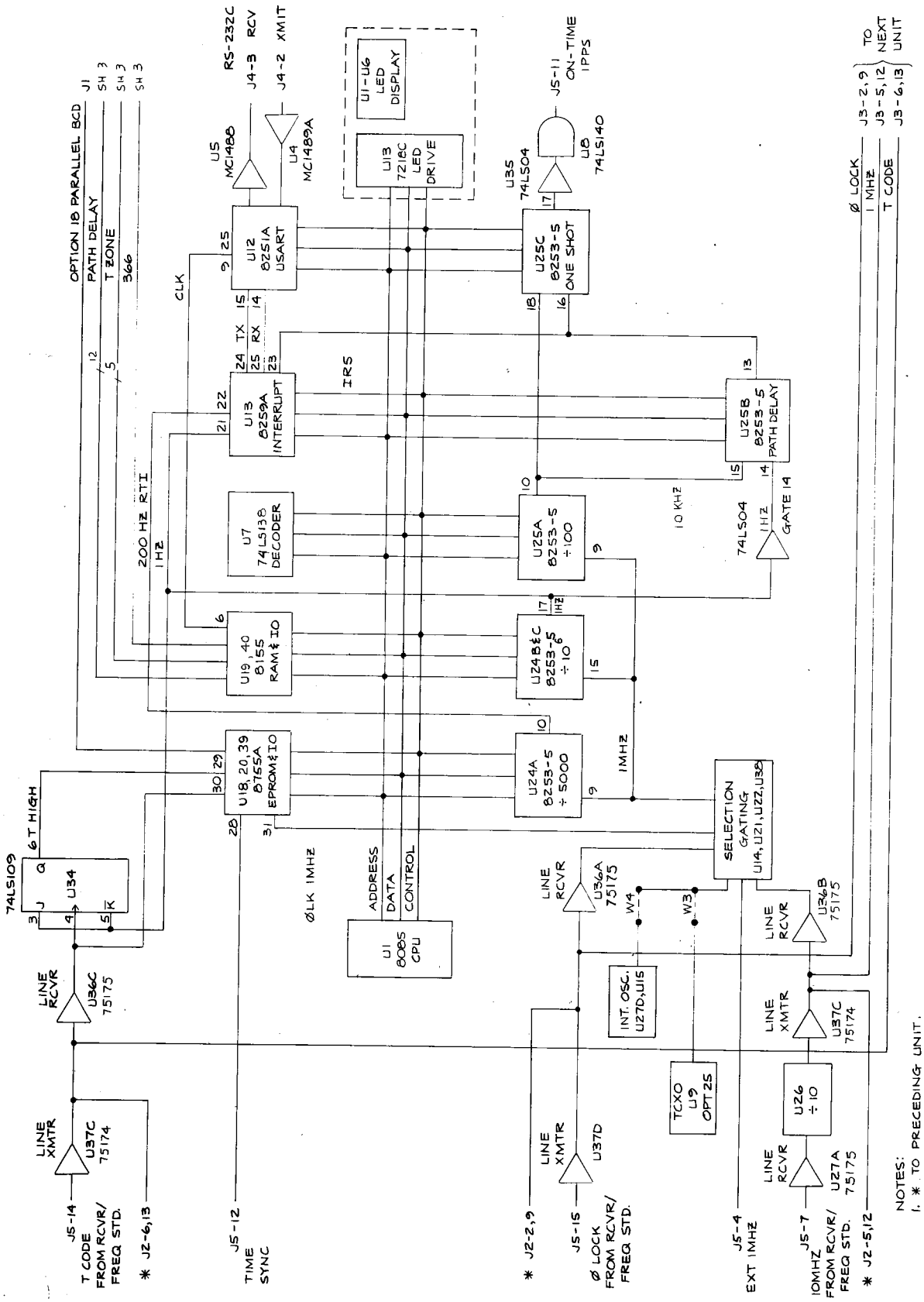


FIG. 2-6 - SCHEMATIC, DC POWER SUPPLY ASSEMBLY



NOTES:
1. * TO PRECEDING UNIT.
2. INSTALL JUMPER W3 OR W4.

FIG. 2-1 MICROPROCESSOR BLOCK DIAGRAM

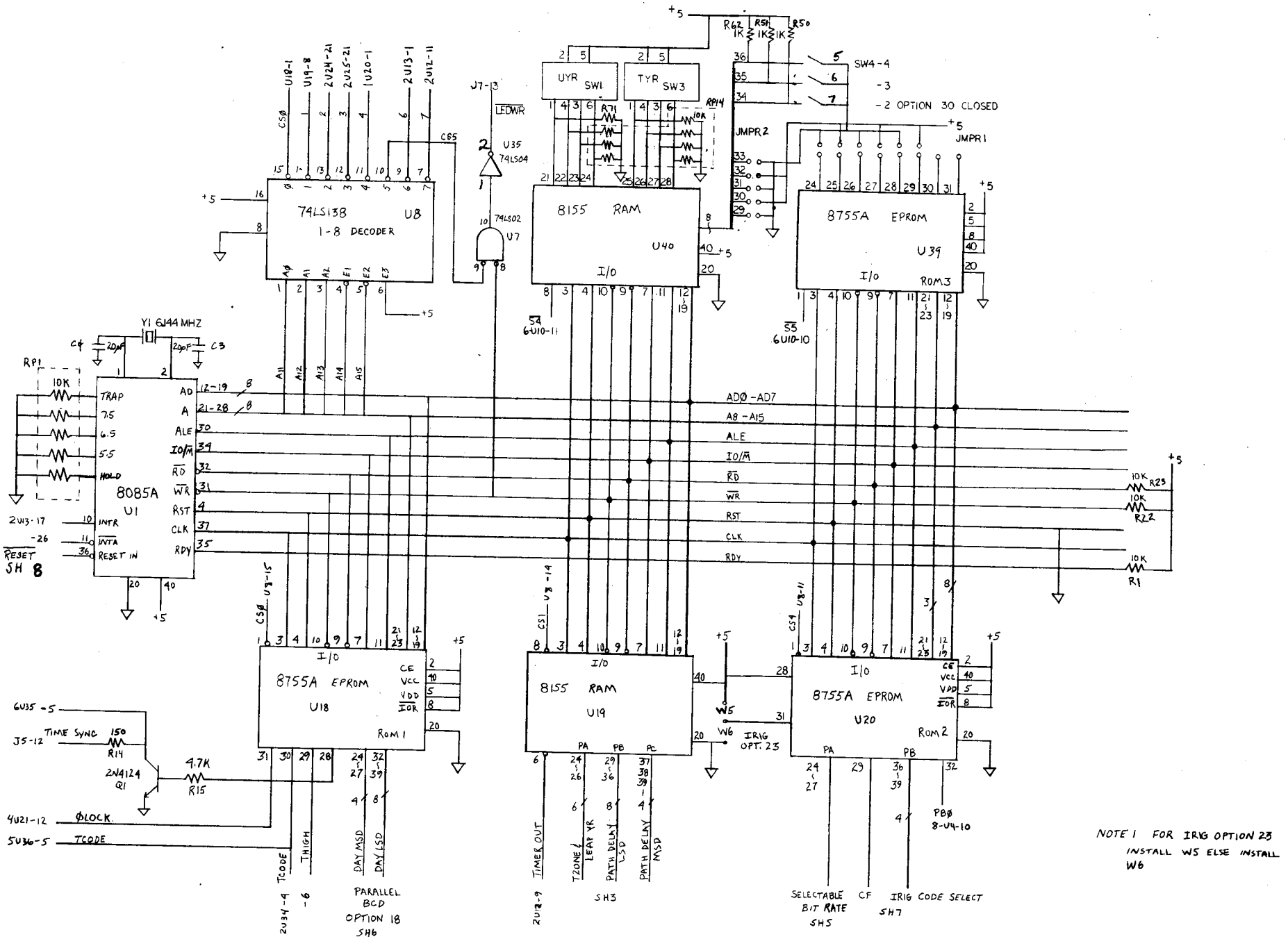
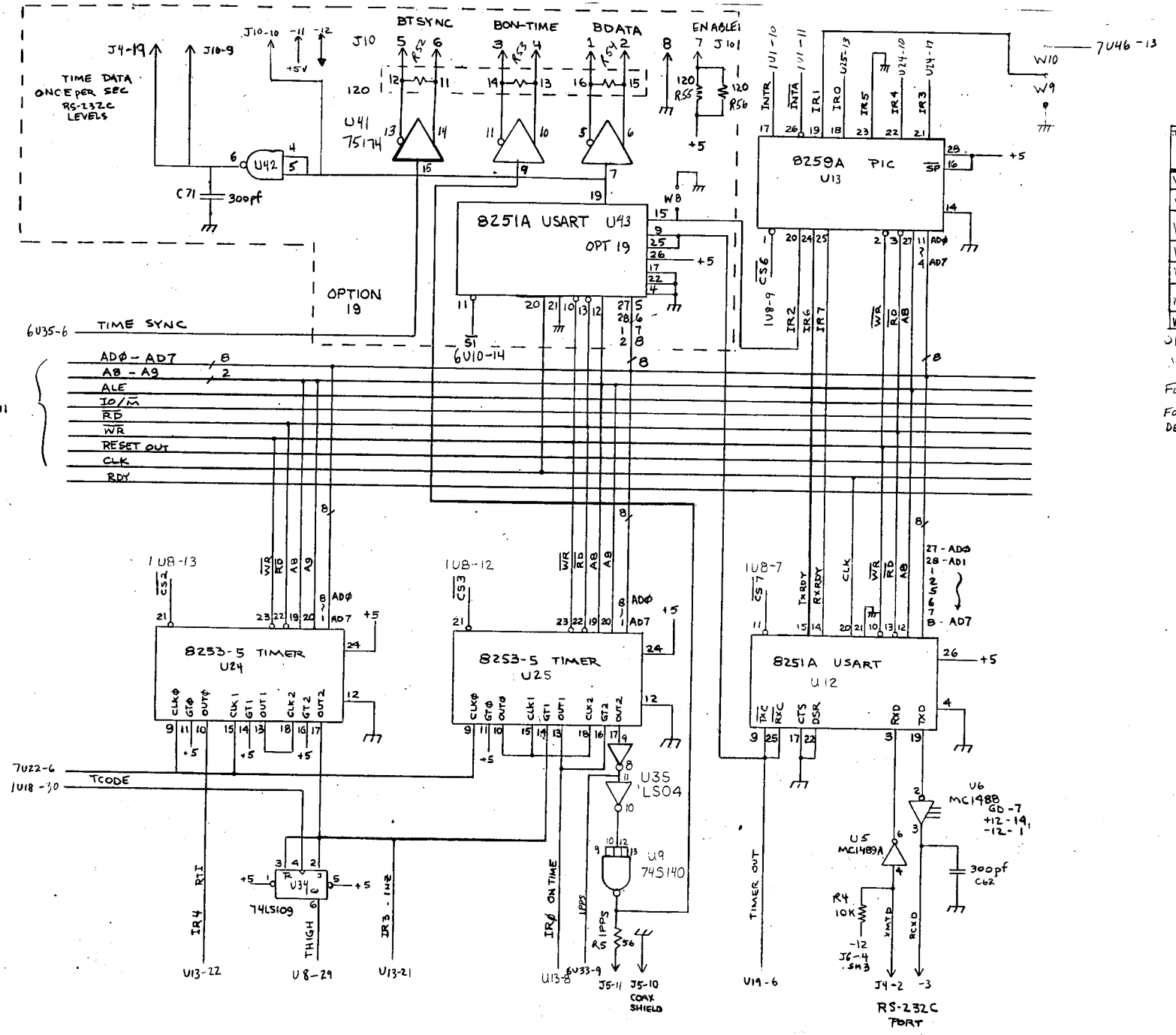


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 1



	OPTIONS							
	STD	19	23	24	19 24	19 24	23 24	ALL OPTIONS
W3	0	0	0	1	0	1	1	1
W4	1	1	1	0	1	0	0	0
W5	0	0	1	0	1	0	1	1
W6	1	1	0	1	0	1	0	0
W8	1	0	1	1	0	0	1	0
W9	1	1	0	1	0	1	0	0
W10	0	0	1	0	1	0	1	1

OPTION 24 ~ DELETE W4 ADD W3

FOR OPTION 19 DELETE W8

FOR OPTION 23, IRIG ADD W10 DELETE W9

FIGURE 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 2

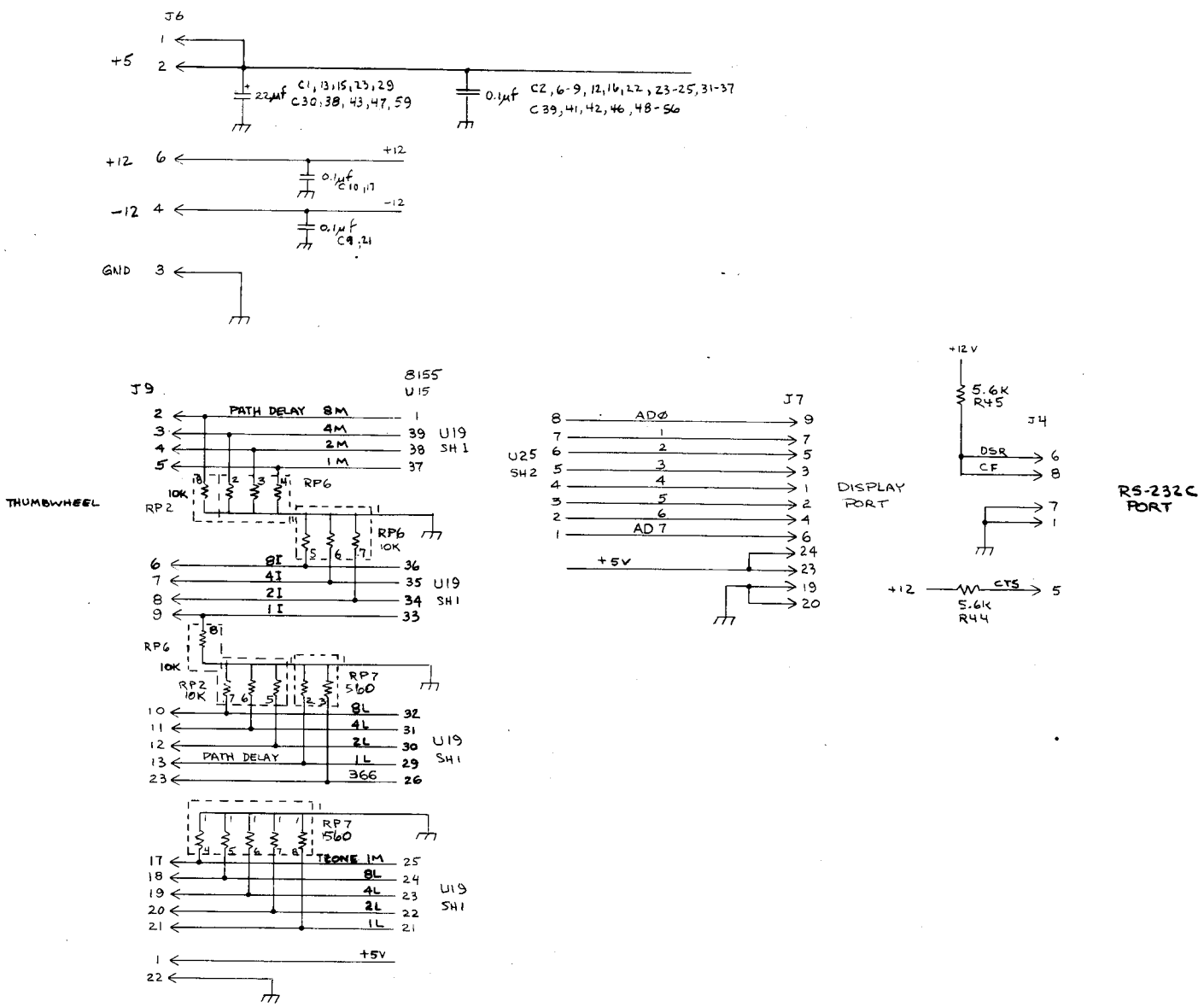
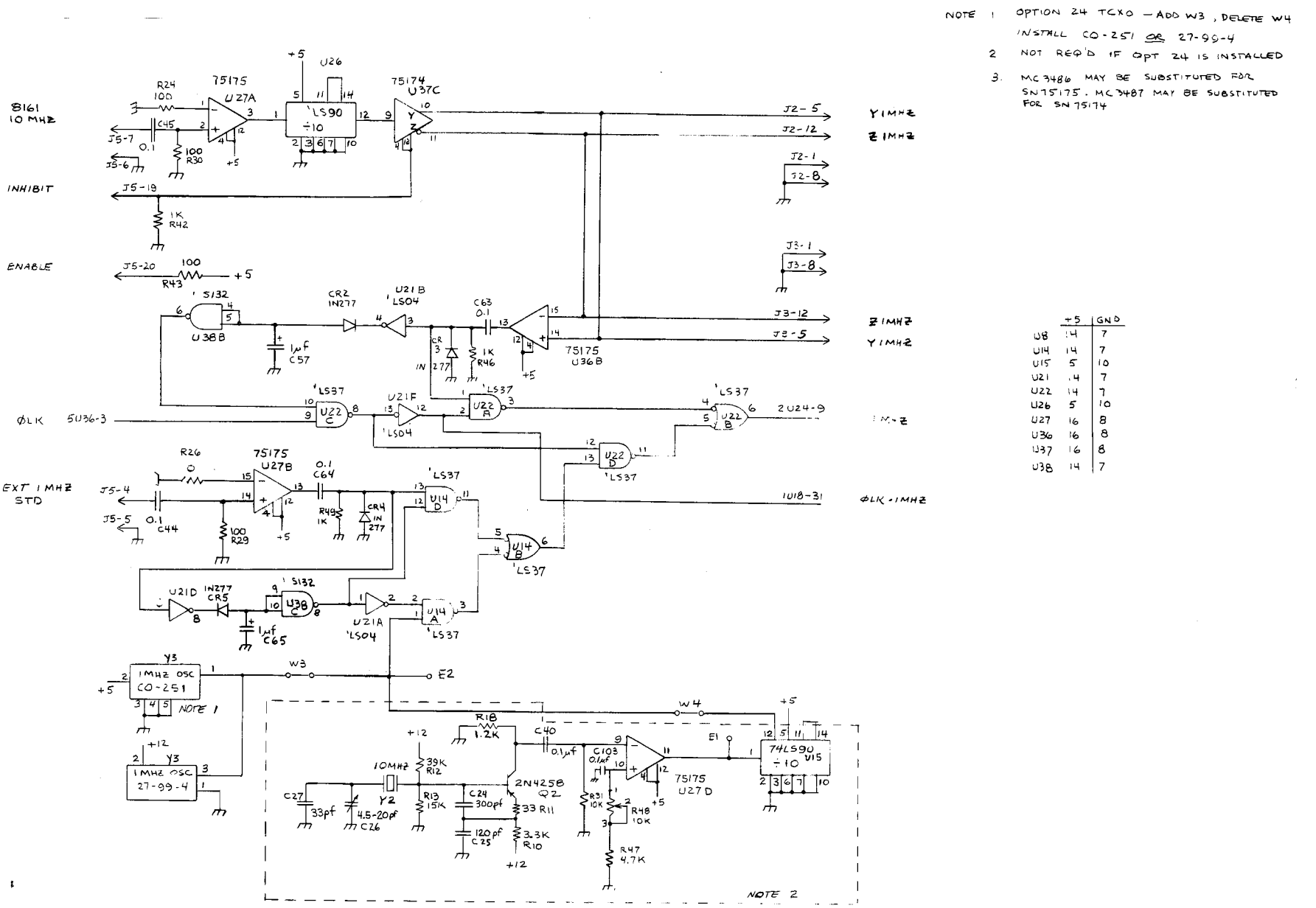


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 3



	+5	GND
U8	14	7
U14	14	7
U15	5	10
U21	14	7
U22	14	7
U26	5	10
U27	16	8
U36	16	8
U37	16	8
U38	14	7

FIGURE 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 4

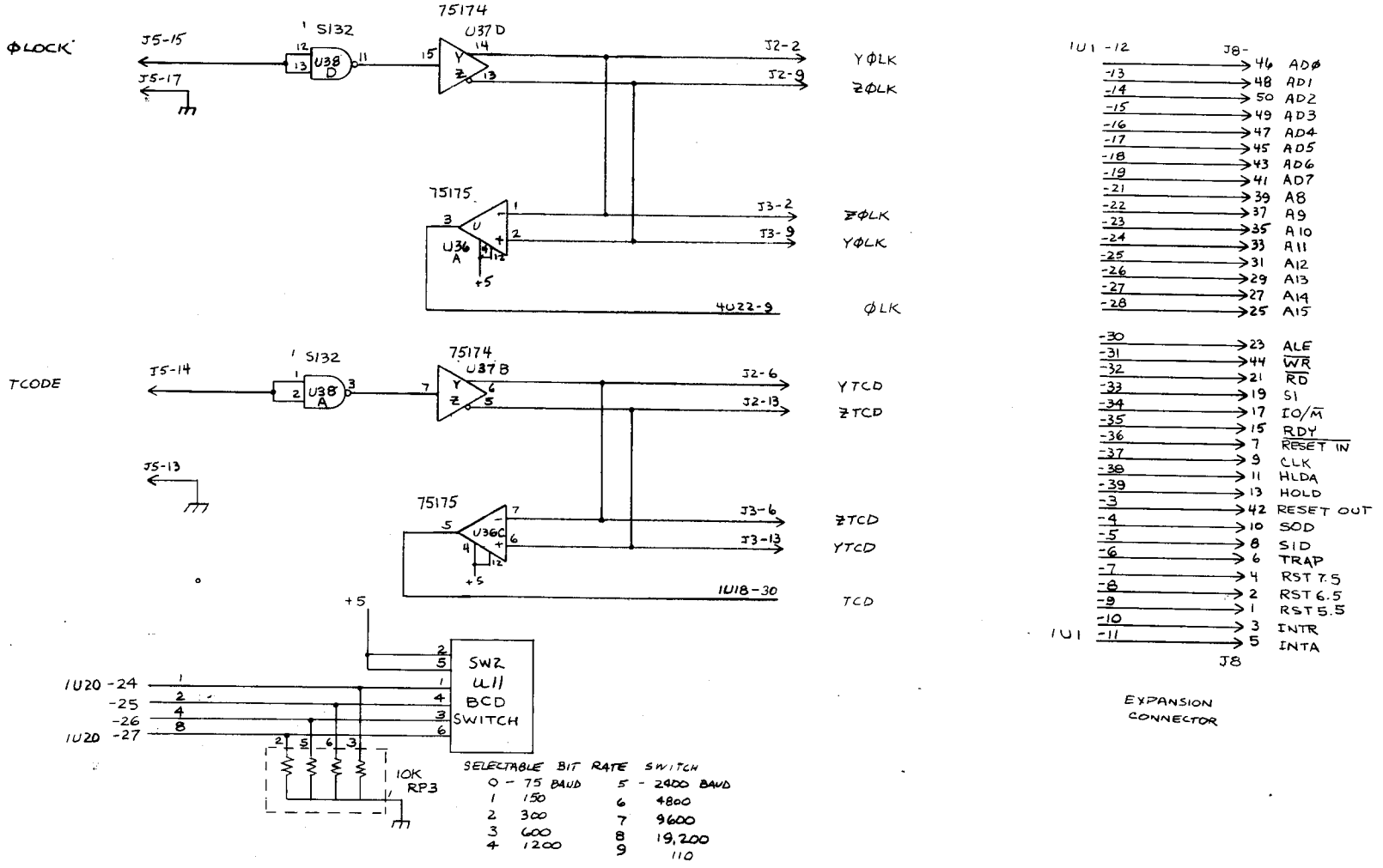
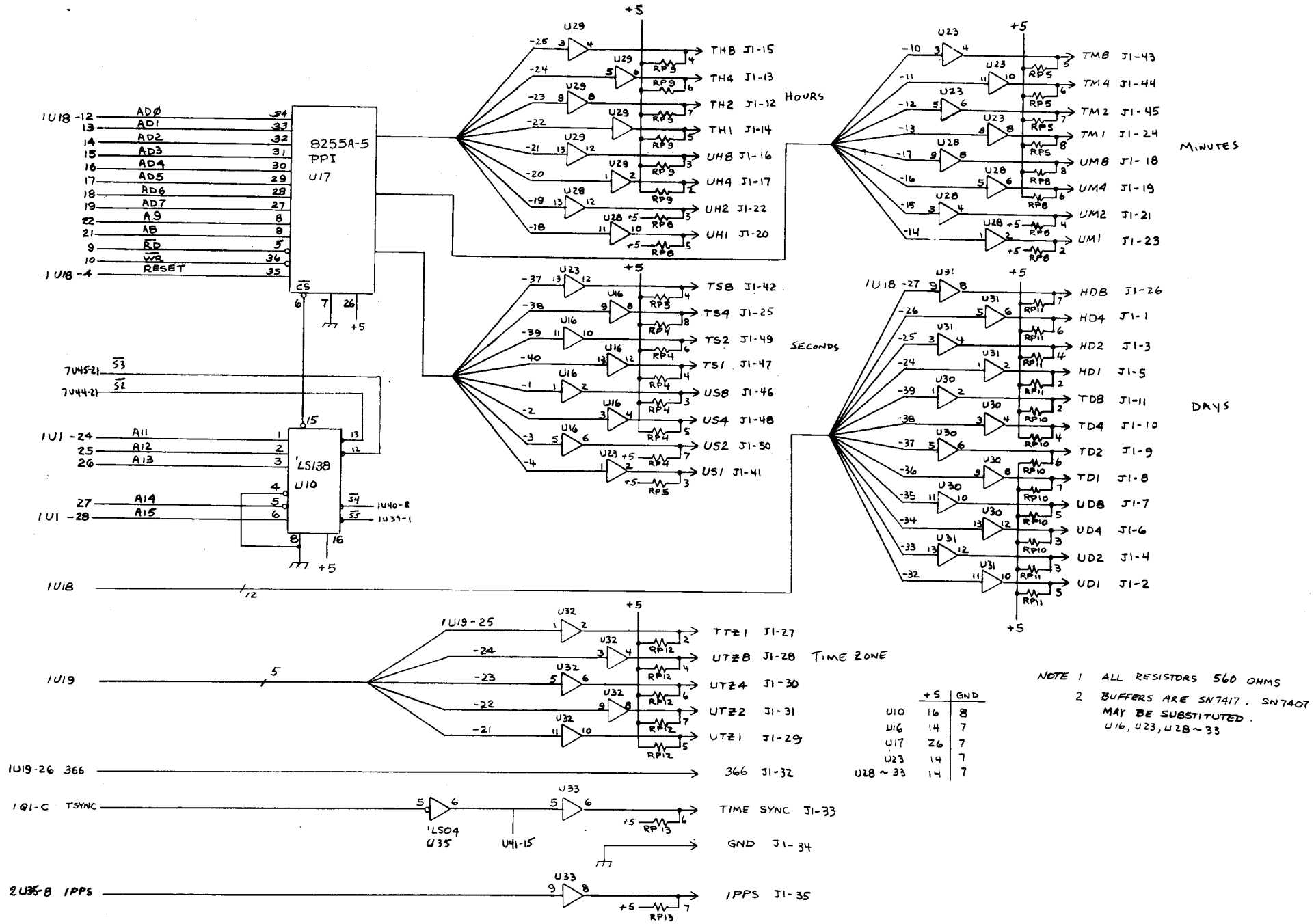


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 5



	+5	GND
U10	16	8
U16	14	7
U17	26	7
U23	14	7
U28 ~ 33	14	7

NOTE 1 ALL RESISTORS 560 OHMS

2 BUFFERS ARE SN7417. SN7407 MAY BE SUBSTITUTED. U16, U23, U28~33

FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 6

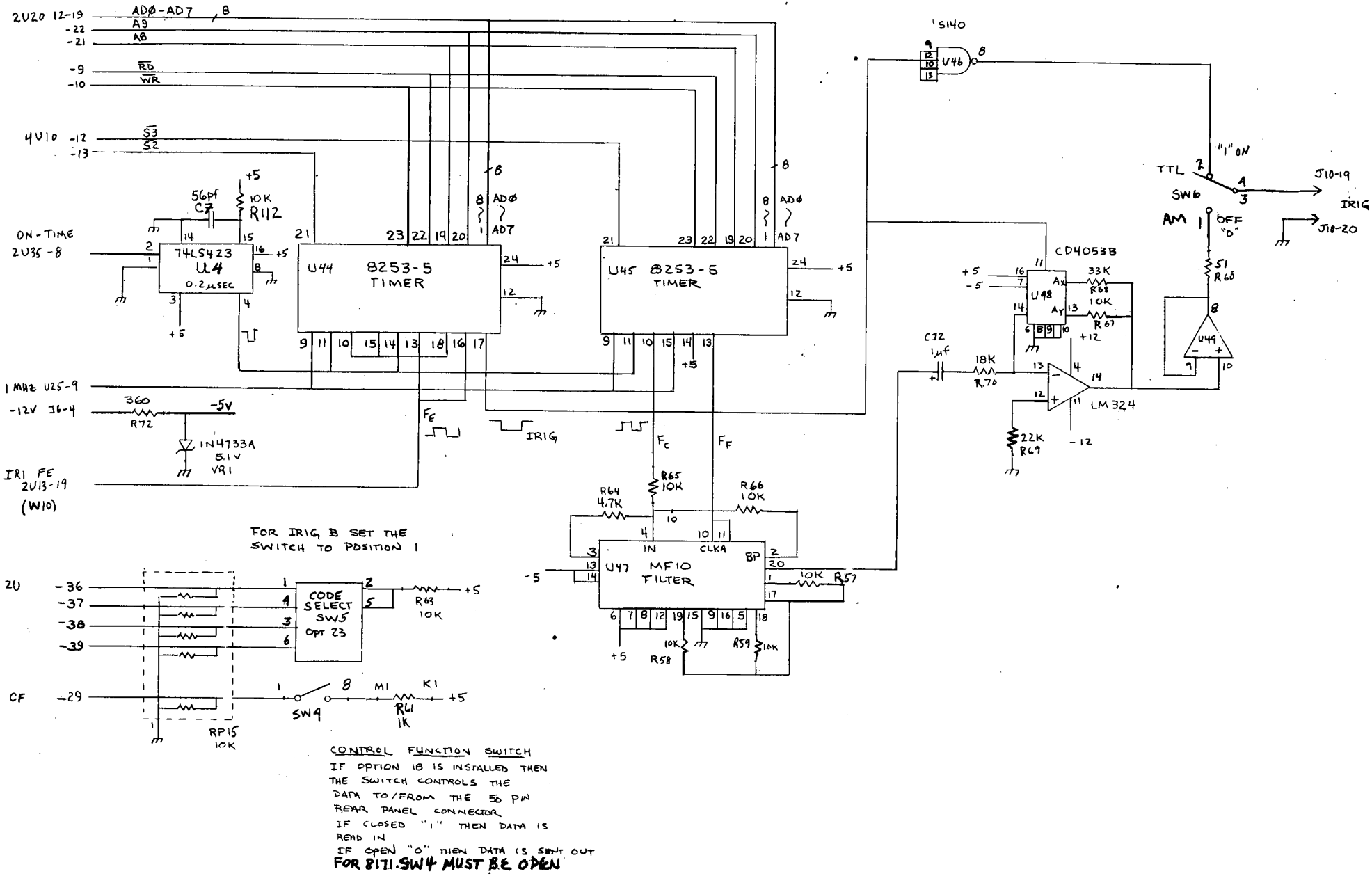


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 7

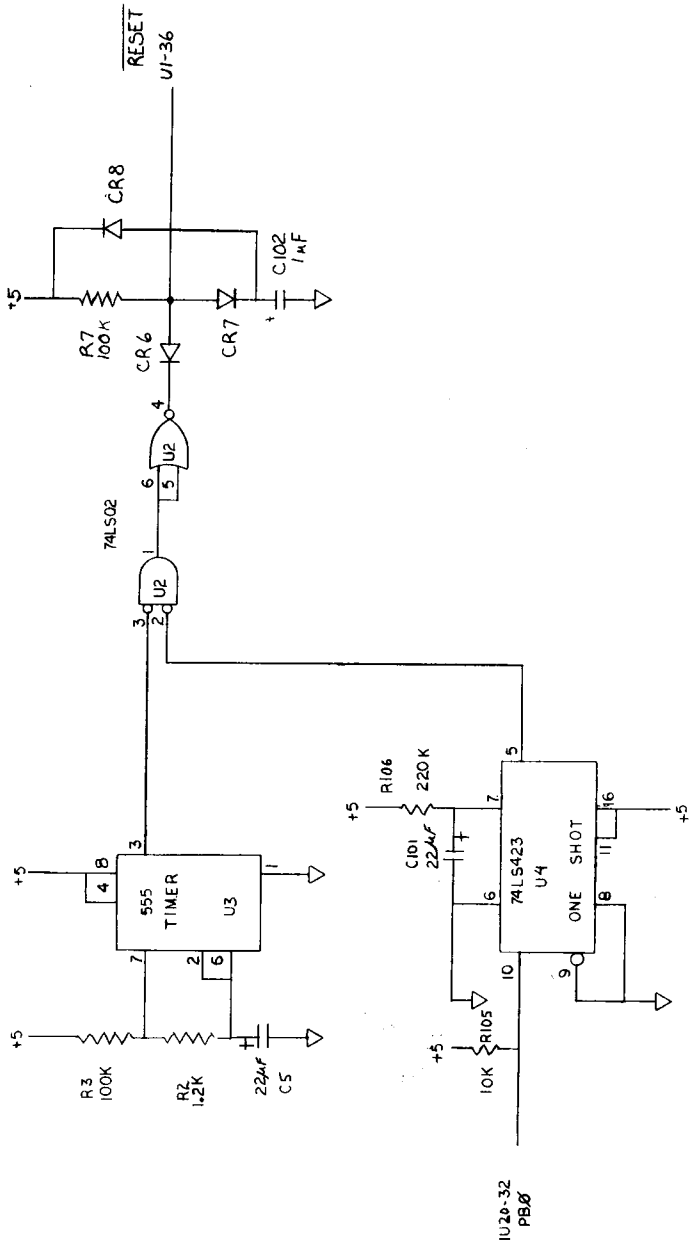


FIG. 2-2 SCHEMATIC - MICROPROCESSOR ASSEMBLY - SHEET 8

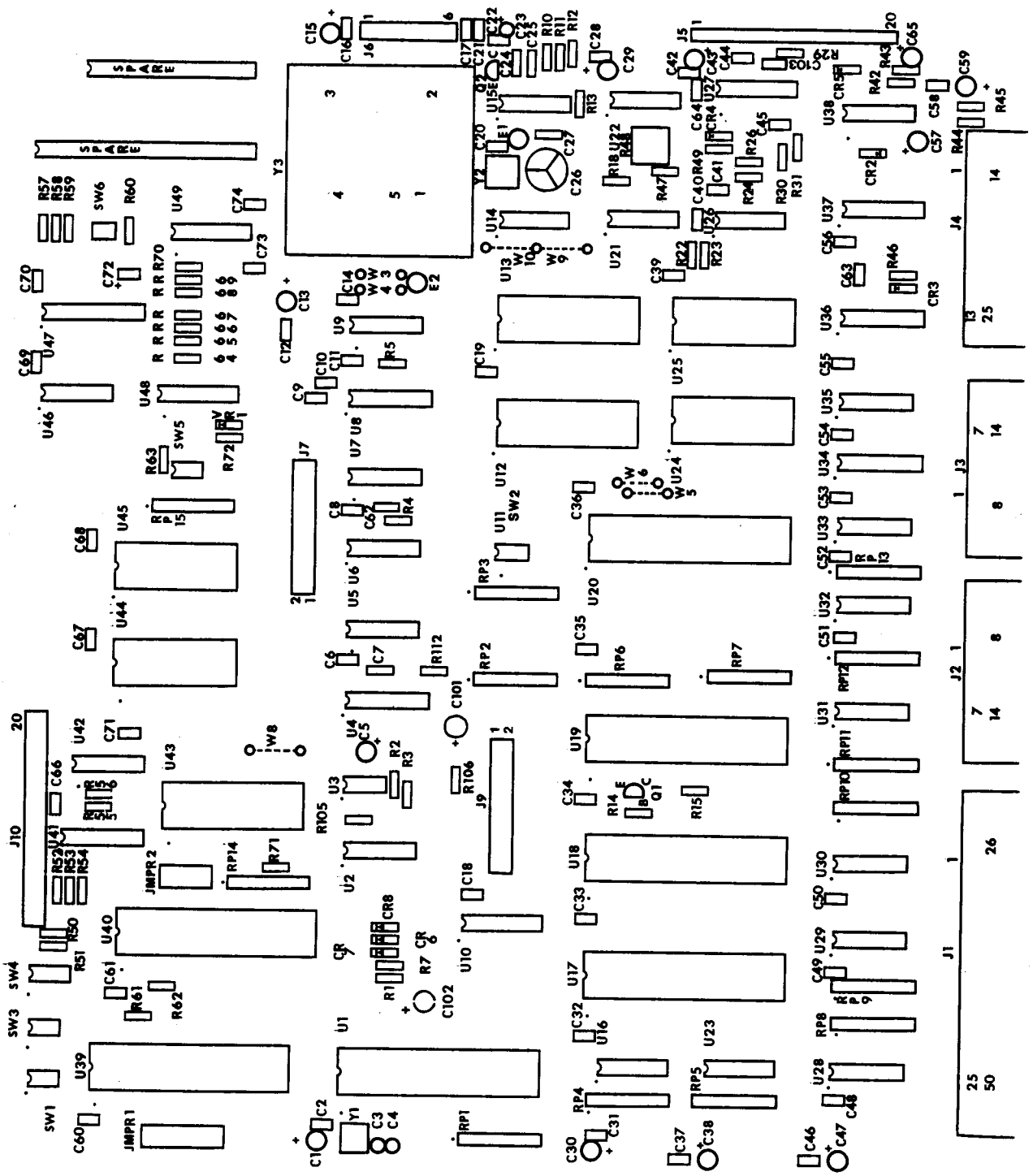


FIGURE 2-3 ASSEMBLY DRAWING - MICROPROCESSOR

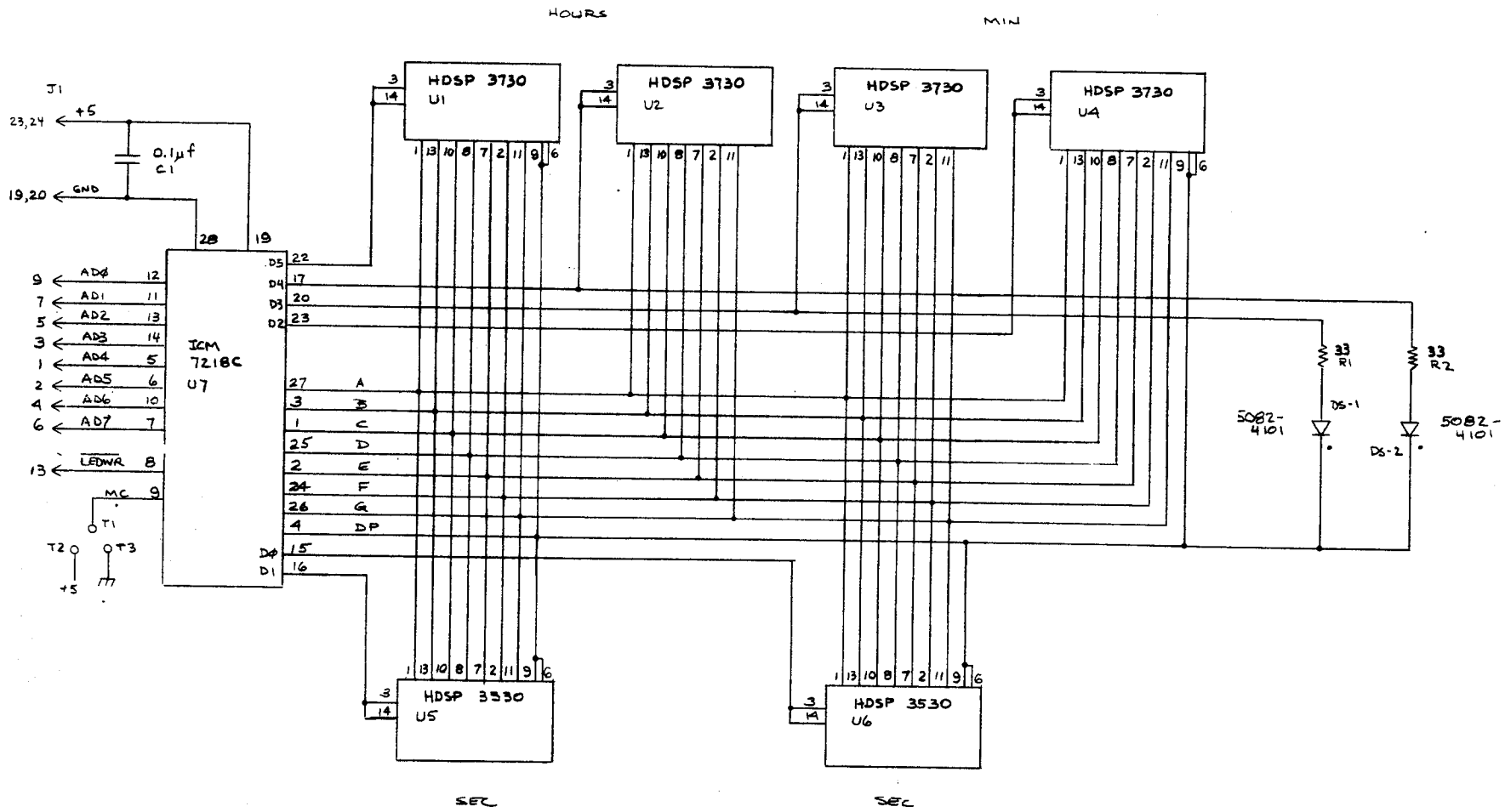


FIG. 2-5 SCHEMATIC, DISPLAY ASSEMBLY

2.4 DC POWER SUPPLY ASSEMBLY, A1A1, P/N 015300

The DC Power Supply Assembly provides +5 VDC, and ±12 volts DC for operation of the Microprocessor and Display Assemblies.

The layout of the DC Power Supply Assembly is shown in Figure 2-6. The schematic is shown is Figure 2-7.

The AC input for the DC power supplies is filtered by capacitors A1C1 and A1C2, then fed through Fuse F1 to transformer A1T1.

The +5 volt DC supply consists of full wave rectifiers, diodes CR1 and CR2, filter capacitors C1 through C7, regulator U1 and Zener diode VR1.

The +12 volt DC supply consists of a bridge rectifier, diodes CR3 through CR6, +12 volt regulator U2, -12 volt regulator U3, and filter capacitors C8 through C15.

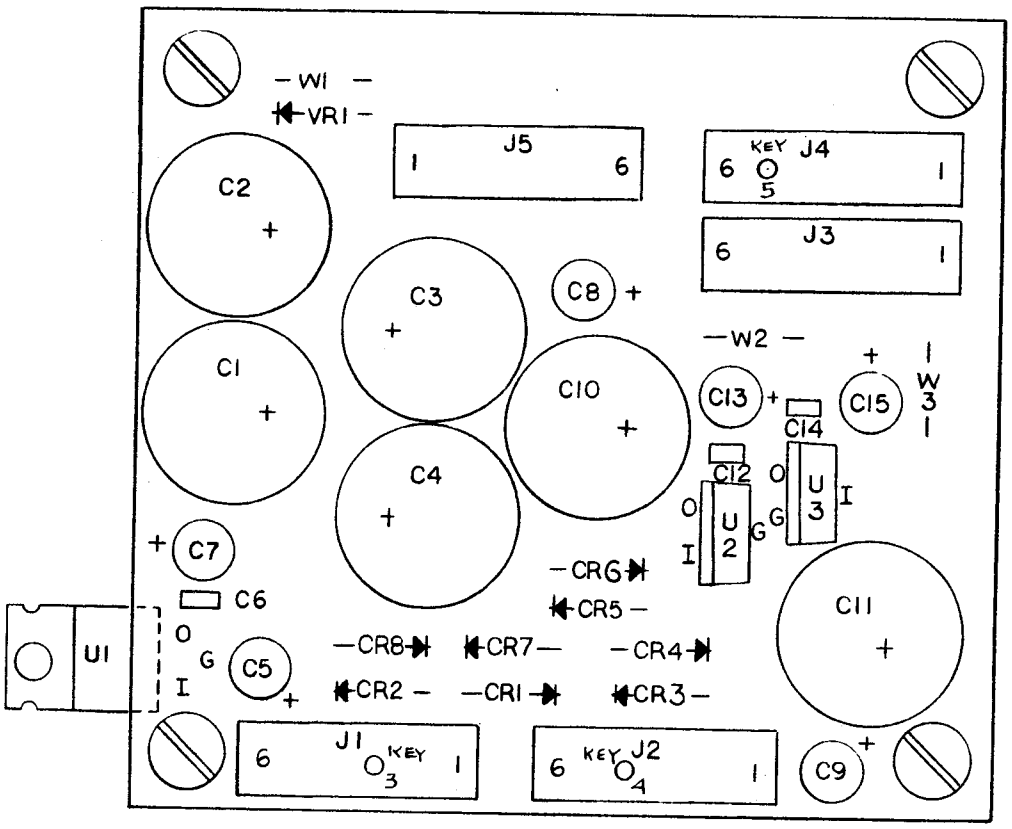


FIG. 2-6 ASSEMBLY DRAWING - DC POWER SUPPLY

SECTION 3

8171A

SERVICE INFORMATION

3.1 Introduction

3.2 Calibration

3.3 Test Equipment

3.4 Test Set-Up

3.5 Test Procedure

3.6 Trouble-shooting

3.1 INTRODUCTION

This section describes how to calibrate, test, and trouble-shoot the Model 8171A. It contains the CALIBRATION procedures, a list of recommended TEST EQUIPMENT, the TEST SET-UP, TEST PROCEDURES, and a TROUBLE-SHOOTING guide.

3.2 CALIBRATION

3.2.1 PATH DELAY AND RECEIVER DELAY CALIBRATION

There are three methods of calibration.

First Method: Provides an absolute accuracy of 5 to 10 milliseconds and does not require a portable clock.

Second Method: Provides a relative accuracy of ±1 millisecond and does not require a portable clock.

Third Method: Provides ±1 millisecond absolute accuracy and requires a portable clock.

First Method: Determine the path delay from Ft. Collins, Colorado, to the receiver location. See the FIG. 1-6 PATH DELAY MAP or use the formula in Section 1.3.8 Propagation Path Delay. Add to this the 17.0 millisecond nominal receiver delay. Set the rear panel thumbwheel switches to the sum of both delays:

Propagation Delay + Receiver Delay = Path Delay Switch Setting

Second Method: This method is recommended for applications that require millisecond accuracy between a group of clocks. Designate one clock as the master clock and calibrate the others against the master. The procedure is:

1. Calibrate the clocks by the First Method.

2. Let them set and run for 2-3 days. The clocks should not lose phase lock during this period. Check the Phase Lock Lost Counter, PLLC, to make sure that the units have not lost phase lock. (See Section 1, Figure 1-4 SAMPLE MEMORY DUMP, for location of PLLC). If phase lock was lost, test should be repeated.

3. Using an oscilloscope or time interval counter, compare the on-time pulse of the unit under test, UUT, against the master clock.

4. Adjust the PATH DELAY thumbwheel switch on the UUT so the time interval between the on-time pulse of the UUT and the master clock is less than 0.1 millisecond.

5. Repeat steps 3 and 4 for each UUT.

6. Wait 24 hours and verify that the on-time pulses are within 1 millisecond.

Third Method: This method requires a portable clock that has been calibrated. The procedure is the same as the Second Method, except the portable clock is used in place of the unit designated as the master clock.

Verification that the clock is on time to the correct second can be made by calling 303-499-7111. The audio portion of WWV signal will be heard. Verify that the clock is set correctly by observing the front panel display.

3.2.2 TIME BASE CALIBRATION

Calibration of the standby 10-MHz crystal oscillator is described in TEST 6. If Option 24 is present, see TEST 10 for calibration of the TCXO. The recommended calibration interval is six months.

3.3 TEST EQUIPMENT

Table 3-1 lists the recommended test equipment for checking the performance of the Model 8171A.

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
WWVB Antenna	60 KHz Active Antenna	Spectracom Model 8206
WWVB Receiver	Same as Model 8161 with Time Code Output	Spectracom Model 8160A, 8161, or 8164 with time code output.
WWVB Clock	Same as Model 8171A	Spectracom Model 8171A
Oscilloscope	2-channel	Tektronix Model 455
Attenuator	50-ohm	--
Voltmeter	4-1/2-Digit Multimeter	Data Precision Model 255
Counter	Accuracy 1 x 10^{-7}	H-P 5315B Universal Counter
TTY	RS-232-C Teletype-writer, buffered. TTY must have a selectable bit rate control.	Teletype KSR43

TABLE 3-1 RECOMMENDED TEST EQUIPMENT

3.4 TEST SET-UP

Install the Model 8161 WWVB Receiver/Oscillator and connect the unit to the Model 8171A with Cable A. The cable plugs into the AUX IN/OUT connector on the rear of the units.

Connect the Standard signal from the front panel of the 8161 through a 50-ohm attenuator to the EXT 1-MHZ INPUT connector on the rear panel of the 8171A. Using a BNC-T connector, connect this signal to Channel B of the oscilloscope.

Connect a buffered RS-232-C teletypewriter to the Serial ASCII port on the rear of the 8171A.

Connect a Bus Terminator (P/N 015500-2) to BUS B connector on the rear of the 8171A.

The connection of the counter, digital multimeter and oscilloscope is specified by the various tests.

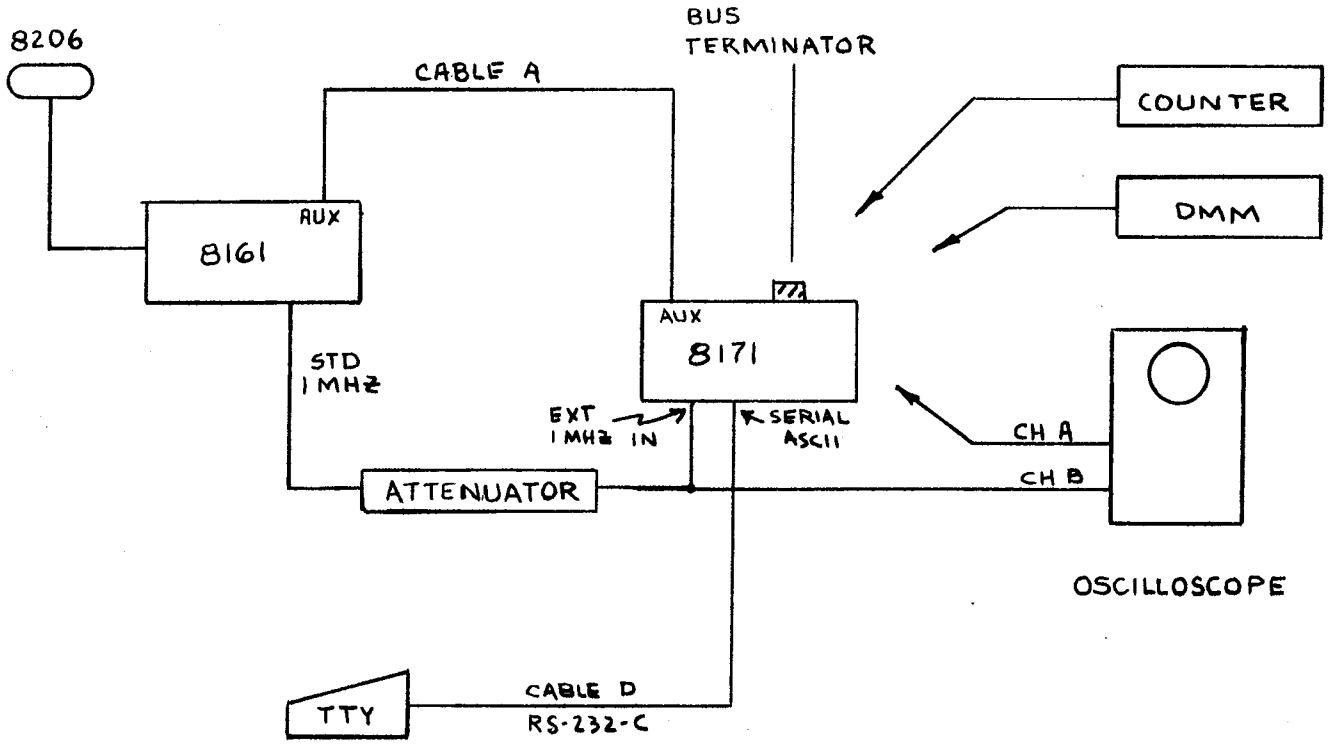


FIGURE 3-1 TEST SET-UP BLOCK DIAGRAM

3.5 TEST PROCEDURE

Reference designations in this section refer to the sheet of the schematic and to component and pin numbers. For example, 1U18-30 refers to pin 30 of integrated circuit U18 found on sheet 1 of the schematic.

TEST 1 - VOLTAGE & FREQUENCY

The purpose of this test is to check the voltages and CPU clock frequency for their correct values.

1U1-40	(+5 ±.25V)	_____V
2U6-14	(+12 ±1.2V)	_____V
2U6-1	(-12 ±1.2V)	_____V
1U1-37	(3.072 ±.03 MHz)	_____MHz

TEST 2 - 8161 INPUT SIGNALS

This test verifies that the signals from the 8161 are received correctly by the 8171A under test. Record the results.

Check that a 1-MHz TTL signal is present at 4U36-13. _____

Check that the ØLOCK signal at 5U36-3 is HIGH if the 8161 is phase locked and LOW when the 8161 is not phase locked. _____

Check that the TCODE signal at 5U36-5 goes high and low when the 8161 is phase locked to WWVB _____

TEST 3 - THUMBWHEEL AND 366/365 SWITCH INPUTS

This test checks the proper operation of the input switches on the rear panel of the 8171A.

Set the clock manually via the TTY or automatically with WWVB.

Advance the TENS and UNITS switches on the TZONE switch and view the front panel display for corresponding changes in the HOUR position of the display.

To check the PATH DELAY switches, synchronize the scope to the positive edge of the 1-Hz reference (2U34-2). Adjust the sweep to 0.1 SEC/CM. Note that the falling edge occurs at the center of the sweep.

Connect a coaxial cable to the 1 PPS ON-TIME connector on the rear panel and observe this signal on the scope. It is a positive-going 100-millisecond pulse that goes high at the center of the sweep (i.e. at the falling edge of the 1-Hz reference.)

Adjusting the PATH DELAY TENS, UNITS and TENTHS switches will move the 1 PPS ON-TIME pulse relative to the 1-Hz reference (2U34-2). The TENS switch will move it 10 milliseconds per digit, the UNITS, 1 millisecond, and the TENTHS, 0.1 millisecond per digit.

Adjust each digit through its range (0-9) and observe that as the switch settings are increased, the ON-TIME pulse moves to the left relative to the 1-Hz reference.

To observe these changes, the delayed sweep capability of the scope should be used.

An alternative test approach is to use the time interval measurement capability of the H-P 5315B counter.

Test the 366/365 switch by observing that 1U19-26 is HIGH when the switch is in the 366 position and LOW when the switch is in the 365 position.

Record the results:

TIME ZONE

TENS _____
UNITS _____

PATH DELAY (2U34-2 REF, VIEW 1 PPS ON-TIME)

TENS _____
UNITS _____
TENTHS _____

366/365 (1U19-26 HIGH/LOW) _____

TEST 4 - TTY COMMANDS

Connect a TTY to the Serial ASCII port and check that the unit responds properly to the T, D, S, and X commands.

Set the switches on the TTY for FULL-DUPLEX and 300 BAUD operation.

Depress "T" and observe that the TTY prints the time message:

DDD HH:MM:SS TZ=XX (without Option 30)
WWW DDMMMYY HH:MM:SS (with Option 30)

Depress "D". The contents of the memory will be printed.

Depress "S111223344". The clock will display the time entered. (Make sure that the TZONE switch is set to 00). Depress "T" and check that the time printed corresponds to the time entered.

Depress "X" (or any other key except T, D, or S). An "*" will be printed.

Record the results:

T (PRINT TIME) _____

D (DUMP MEMORY) _____

S (SET TIME) _____

X (PRINT *) _____

TEST 5 - OUTPUTS

Measure the parameters of the 1 PPS ON-TIME pulse on the rear panel connector.

Verify that the TSYNC LED on the front panel comes on when the clock sets itself and stays on for 10 minutes after the antenna is disconnected, provided SW4-3,4 are both set OFF ("0").

Check the display to see that all digits and the colon are operating properly.

1 PPS ON-TIME (Rear Panel BNC)
- FREQ (1 HZ) _____HZ
- AMPLITUDE (TTL) _____V
- PULSE WIDTH (0.1 SEC) _____

TSYNC LED (ON/OFF) _____

DISPLAY & COLON _____

TEST 6 - 10-MHZ STANDBY OSCILLATOR

This test checks the tuning range of the 10-MHz crystal oscillator and adjusts it to within $\pm 1 \times 10^{-6}$.

Observe the 10-MHz signal at 4U27-11. Adjust potentiometer 4R48 for a square wave. Glyptol the potentiometer.

Measure the tuning range of the oscillator by adjusting 4C60.

Set the frequency of the oscillator to within 10.0 MHz ±5 Hz.

Record the results:

4U27-11 (TTL 10-MHz Square Wave) _____

MIN FREQUENCY 9,999,700 _____Hz

MAX FREQUENCY 10,000,100 _____Hz

SET FREQUENCY 10,000,000 ±5 _____Hz

TEST 7 - EXT 1-MHZ INPUT

This test checks the input sensitivity of the EXT 1-MHZ INPUT.

Connect a 50-ohm attenuator between the 1-MHz standard and the EXT 1-MHZ INPUT connector on the rear panel.

Adjust the attenuator for 1 volt peak-to-peak output (0.35V RMS).

Observe 4U27-13 for a TTL Output. _____

TEST 8 - 1-MHZ TIME BASE SELECTION

The purpose of this test is to verify that the proper 1-MHz time base is selected.

TEST	ØLOCK AND 1 MHZ 4U22-8	EXT 1-MHZ INPUT 4J5-4	1-MHZ SELECTED 4U22-6	TEST RESULTS
8A	1	1	VCXO (8161)	_____
8B	1	0	VCXO (8161)	_____
8C	0	1	EXT 1-MHz Input	_____
8D	0	0	TCXO - Opt. 24 or XTAL OSC	_____

TEST 8A. Connect the unit as shown in Figure 3-1, TEST SET-UP BLOCK DIAGRAM. Connect Channel A of the scope to 4U22-6. Obtain phase lock to WWVB. The signal at 4U22-6 is a 1-MHz signal with a 1 to 3 microsecond jitter.

The source of the signal is the VCXO in the 8161. The jitter is a function of the signal-to-noise ratio at the antenna of the receiver.

TEST 8B. Disconnect the EXT 1-MHZ INPUT signal and observe that the signal at 4U22-6 remains unchanged.

TEST 8C. Disconnect the 8206 antenna and connect the EXT 1-MHZ INPUT. Wait until the phase lock is lost (about 30 seconds). The signal at 4U22-6 will not jitter or drift. It is derived from the same signal that is on the other channel and is synchronizing the scope.

TEST 8D. Disconnect the EXT 1-MHZ INPUT. The signal at 4U22-6 will be the 1-MHz signal derived from the TCXO if Option 24 is present. If Option 24 is not installed it will be the local 10-MHz crystal oscillator. The signal observed will drift relative to the 1-MHz standard synchronizing signal.

TEST 9 - DAISY CHAIN TEST

This test is to be performed only if the system consists of more than one 8171A. The purpose of this test is to check that the 8171A under test will work when connected in other than the first position.

Connect the 8171A under test in position 2. Refer to Fig. 1-3, SYSTEM CONFIGURATION. Terminate the chain with a BUS TERMINATOR (P/N 015500-2).

Observe the LED front panel display for proper operation.

Record the results: OPERATION CORRECT _____

TEST 10 - PERFORMANCE

This test measures the system performance. The parameter measured is the number of good time codes received over a given time interval.

Install the 8206, 8161, and 8171A per installation instruction in each manual. After the time has been set, dump the memory using the "D" command and record the contents of the TIME CODE COMPARE COUNTER, TCCC. Section 1 of this manual describes the location and interpretation of this counter.

Wait 20 minutes and again dump the memory and read the TCCC.

Convert the readings from HEXIDECIMAL to DECIMAL. Subtract the earlier reading from the later, and divide the results by the time interval in minutes between dumps. This number is the good compare rate.

$$\text{GOOD COMPARE RATE} = \frac{TCCC_1 - TCCC_2}{(\text{delta})t}$$

This rate will vary as a function of received signal-to-noise ratio. During periods of good reception it will nominally be greater than 50%. During periods of poor signal-to-noise ratio, the good compare rate over a 20-minute interval may be zero. If so, repeat the test over a 24-hour period. The longer averaging period tends to mask out short periods of atmospheric disturbance.

Record the results: RATE _____%

TEST 11 - OPTION 18 - PARALLEL BCD

The purpose of this test is to verify that all output signals will go high and low.

Using the TTY, enter the SET COMMAND "S777777777". This will set the clock to all sevens. Observe Hours, Minutes and Seconds parallel BCD outputs for 7's (Binary 0111) output on each of the BCD digits. Set the clock to "S888888888" and observe the BCD outputs for 8's (Binary 1000). Because the clock continues to run it is necessary to use the SET COMMAND again during the test of the seconds and minutes.

To test the TZONE outputs adjust the TZONE switch to 07 and observe the outputs for proper levels. Next, adjust the TZONE switch to 18 and observe the outputs.

To test the 366/365 function, observe that the signal at 6J1-32 is high when the switch is in the 366 position and low when the switch is in the 365 position.

To test the TIME SYNC function, 6J1-33, obtain Time Sync and observe that the signal is high.

To test the TIME SYNC signal for the low condition, momentarily remove power from the 8171A under test. The signal at 6J1-33 should be low when power is reapplied.

The last signal to test is the 1 PPS signal at 6J1-35. Observe that it is a positive-going 100-millisecond TTL pulse that occurs once per second.

Record the results. S777777777/S888888888 TZ = 00

PIN	LEVEL		PIN	LEVEL		PIN	LEVEL	
1	HD4	1/0 ____	17	UH4	1/0 ____	33	TSYNC	____
2	UD1	1/0 ____	18	UM8	0/1 ____	34	GND	____
3	HD2	1/0 ____	19	UM4	1/0 ____	35	1 PPS	____
4	UD2	1/0 ____	20	UH1	1/0 ____	36 to 40	open	
5	HD1	1/0 ____	21	UM2	1/0 ____	41	US1	1/0 ____
6	UD4	1/0 ____	22	UH2	1/0 ____	42	TS8	0/1 ____
7	UD8	0/1 ____	23	UM1	1/0 ____	43	TM8	0/1 ____
8	TD1	1/0 ____	24	TM1	1/0 ____	44	TM4	1/0 ____
9	TD2	1/0 ____	25	TS4	1/0 ____	45	TM2	1/0 ____
10	TD4	1/0 ____	26	HD8	0/1 ____	46	US8	0/1 ____
11	TD8	0/1 ____	27	TTZ1	1/0 ____	47	TS1	1/0 ____
12	TH2	1/0 ____	28	UTZ8	0/1 ____	48	US4	1/0 ____
13	TH4	1/0 ____	29	UTZ1	1/0 ____	49	TS2	1/0 ____
14	TH1	1/0 ____	30	UTZ4	1/0 ____	50	US2	1/0 ____
15	TH8	0/1 ____	31	UTZ2	1/0 ____			
16	UH8	0/1 ____	32	366/365	____			

TEST 12 - OPTION 24 - TCXO CALIBRATION

The purpose of this test is to set the 1-MHz TCXO to within $\pm 1 \times 10^{-7}$ of the 1-MHz standard.

Connect the 1-MHz standard to Channel B of the scope. With the scope synchronized to the standard, observe the 1-MHz signal at test point 4E2. It will drift with respect to the standard. Remove the screw from the side of the TXCO and with a non-metallic screwdriver, adjust the oscillator for minimum drift.

Record the frequency drift. _____usec/second

A drift of 0.5 useconds in 5 seconds is 1×10^{-7}.

TEST 13 - SELECTABLE BIT RATE

Selectable Bit Rate provides 10 selectable bit rates. Connect the TTY to the Serial ASCII port and display the time message at each bit rate.

The baud rate is selected by SW2 in location 5U11.

SW SETTING			SW SETTING		
0	75 baud	____	5	2400 baud	____
1	150 baud	____	6	4800 baud	____
2	300 baud	____	7	9600 baud	____
3	600 baud	____	8	19200 baud	____
4	1200 baud	____	9	110 baud	____

3.6 TROUBLE-SHOOTING

The approach to trouble-shooting is to isolate the problem to the unit, then isolate the problem to the subassembly, then isolate the problem to the component.

Install the unit in the test set-up described in paragraph 3.4 of this section.

ISOLATE TO 8171A - Perform TEST 2, 8161 INPUT SIGNALS, to determine if the 8171A under test has the proper input signals. If the incoming signals are good, then continue with the next step. If TEST 2 fails, then trace the missing signal(s) until the malfunction is found.

ISOLATE TO POWER SUPPLY BOARD - Perform TEST 1, VOLTAGE & FREQUENCY. If the proper voltages are present, then the power supply assembly and interconnections up to the test points are satisfactory. If the voltages are incorrect, disconnect the power cable (A1A2-J6) and measure the voltages at the output pins on the power supply board with reference to ground (A1A1J4-3).

A1A1J4-1	5V ±.25	_____VDC
A1A1J4-6	+12V ±1.2	_____VDC
A1A1J4-4	-12V ±1.2	_____VDC

If all the voltages are correct, then the power supply subassembly is functioning properly. If the voltages are not correct, then trouble-shoot the power supply board using the schematic and assembly drawing in Section 2.

ISOLATE TO MICROPROCESSOR BOARD - The person trouble-shooting the microprocessor board should be familiar with microprocessors and with the operation of the integrated circuits used on the board.

The highest failure rate components are the sockets and connectors. Visually inspect each socket and connector.

Using the oscilloscope, observe the output of the dividers for the proper frequencies:

2U24-9	1 MHz	_____
2U24-10	200 Hz	_____
2U25-17	1 Hz	_____
2U25-10	10 KHz	_____
4U15-12	1 MHz	_____
4U26-12	1 MHz	_____

The time base select logic shown on sheets 4 and 5 of the schematic can be checked by probing for the levels and signals described in Section 2.

Missing BCD output (Option 18) bits can be traced through the buffering shown on Fig. 2-2 sheet 6 in Section 2.

Check each signal on the 8085A CPU (1U1). Because many of the signals are tri-state and not periodic, the determination of what is good and bad is difficult, but signals that are latched high or low can easily be identified.

If the trouble cannot be isolated by testing, then substitute a good 8085A CPU chip for the one under test. Continue substituting IC chips except for the EPROM chips in location 1U18 and 1U20.

If the trouble cannot be isolated and repaired, phone the factory (716-381-4827) for assistance.

SECTION 4

MODEL 8171A

OPTIONS

4.1	Option 18	Parallel BCD Output
4.2	Option 19	Remote Output Driver
4.3	Option 23	IRIG B Output
4.4	Option 24	TCXO
4.5	Option 30	Fully Decoded Text Stream

4.1.0 OPTION 18 - PARALLEL BCD OUTPUT

The Parallel BCD Option provides the day and time data in parallel BCD format on a 50-pin connector. All lines are TTL-compatible. Data is valid 20 milliseconds before the ON-TIME pulse and remains valid until 850 milliseconds after the ON-TIME pulse.

There will be no data out until the clock has been set by WWVB or by the manual SET command.

All signals are positive logic: a logical 1 is a high, a logical 0 is a low.

The signal names and pin numbers are listed below. 8-4-2-1 BCD weighting is indicated in the mnemonic.

SIGNAL	MNEMONIC	PIN
Hours MSD	TH8	J1-15
"	TH4	J1-13
"	TH2	J1-12
"	TH1	J1-14
Hours LSD	UH8	J1-16
"	UH4	J1-17
"	UH2	J1-22
"	UH1	J1-20
Minutes MSD	TM8	J1-43
"	TM4	J1-44
"	TM2	J1-45
"	TM1	J1-24
Minutes LSD	UM8	J1-18
"	UM4	J1-19
"	UM2	J1-21
"	UM1	J1-23
Seconds MSD	TS8	J1-42
"	TS4	J1-25
"	TS2	J1-49
"	TS1	J1-47
Seconds LSD	US8	J1-46
"	US4	J1-48
"	US2	J1-50
"	US1	J1-41
Days MSD	HD8	J1-26
"	HD4	J1-1
"	HD2	J1-3
"	HD1	J1-5

SIGNAL	MNEMONIC	PIN
Days ISD	TD8	J1-11
"	TD4	J1-10
"	TD2	J1-9
"	TD1	J1-8
Days LSD	UD8	J1-7
"	UD4	J1-6
"	UD2	J1-4
"	UD1	J1-2
Time Zone MSD	TTZ1	J1-27
Time Zone LSD	UTZ8	J1-28
"	UTZ4	J1-30
"	UTZ2	J1-31
"	UTZ1	J1-29
Leap Year Switch	366	J1-32
Time Sync	Time Sync	J1-33
Ground	GND	J1-34
On-Time Pulse	1PPS	J1-35

A high on the leap year switch (366) indicates that the switch is set for leap year and day 365 will roll over to 366 instead of to day 1.

The time data is valid when the TIME SYNC signal is high. The leading edge of the ON-TIME PULSE is the on-time point. The pulse has a 10% duty cycle.

4.1.1 OPTION 18 - PRINCIPLES OF OPERATION

The schematic for Option 18 is sheet 6 of Figure 2-2. The assembly drawing is Figure 2-3.

The HOURS, MINUTES and SECONDS are fed out by U7, a Programmable Peripheral Interface integrated circuit. The DAYS data are fed from U18. All signals except the 366/365 are fed through non-inverting buffers.

Other signals brought out are:

366/365 - High if leap year switch is in position 366, otherwise low.

TIME SYNC - High if TIME SYNC LED on front panel is ON else it is low.

GND - Ground

1 PPS - The ON-TIME pulse that occurs once per second.

4.1.2 OPTION 18 - PERFORMANCE CHECKS

To verify the proper operation of Option 18, connect an RS-232C terminal to the Model 8171A WWVB Synchronized Clock. Adjust the TIME ZONE switch on the rear panel to zero.

Using the RS-232C terminal, manually set the clock to all 7's. The SET command is S777777777. This results in a BCD word for each digit of 0111. Verify that the output levels on the Option 18 Parallel BCD connector are proper.

Manually set the clock to all 8's. The SET command is S888888888. This results in a BCD word for each digit of 1000. Verify that this is true. Note that the seconds digits are changing, some interpolation is required for the seconds digits.

This test verifies that the DDD HH:MM:SS signals can be driven HIGH and LOW.

Check the levels of the TIME ZONE signals by first setting the TIME ZONE thumbwheel switch on the rear panel to 07 and measure the outputs, then setting the switch to 18 and measure the outputs for proper value.

Install the Auxiliary IN/OUT interface connector from a Model 8161 to the rear panel of the Model 8171A. Before the clock sets, observe that the TIME SYNC signal out of the Option 18 connector is LOW. Obtain TIME SYNC. Observe that the TIME SYNC signal goes HIGH.

Check the ON-TIME pulse. Monitor with an oscilloscope and observe that it is a TTL signal that occurs once per second and has a 10 duty cycle. The leading edge is the ON-TIME point.

4.2.0 OPTION 19 - REMOTE OUTPUT DRIVER

Option 19 is standard on units with serial numbers 8171-0566 and higher. The Spectracom Model 8171A WWVB Synchronized Clock receives and decodes the time signal transmitted by the National Bureau of Standards at Ft. Collins, Colorado. Option 19 Remote Output Driver provides a method of distributing this data to multiple remote locations. Once-per-second a string of ASCII characters that contain day-of-year, time-of-day, and time zone setting information are sent on the bus. An on-time pulse and a time sync status signal is also

transmitted. The electrical characteristics of the data signals conform to the EIA RS-422 standard. Up to 32 receivers may be employed at distances up to 4000 feet. If Option 30, Fully Decoded Text Stream, is present, the day of the week, month and year are transmitted. The day of the year (1-366) and TIME ZONE switch setting is not transmitted.

The Spectracom Model 8173 Multiple RS-232C Tap may be connected to the Remote Output bus. Model 8173 provides four RS-232C ports for easy interfacing to computer systems. Up to 32 Model 8173's may be connected to the bus.

An unlimited number of ports may be obtained by using the buffered output bus on the Model 8173. This port regenerates the data and provides another set of RS-422 drivers that can drive up to 32 loads at 4000 feet.

The Spectracom Model 8172 Remote Clock may be connected to Option 19 Remote Output Driver. Model 8172 is a digital wall clock that provides an HOURS, MINUTES, SECONDS 12- or 24-hour display.

The time data are also brought out as an RS-232C signal on both the Remote Output connector pin 5 and the Serial ASCII connector pin 19.

4.2.1 OPTION 19 - SPECIFICATIONS

Output Connector - The Remote Output Connector is a 9-pin series D receptacle (female). The Serial ASCII output connector is a 25-pin series D receptacle. Figure 4-1 shows the pin locations viewed from the rear of the Model 8171A.

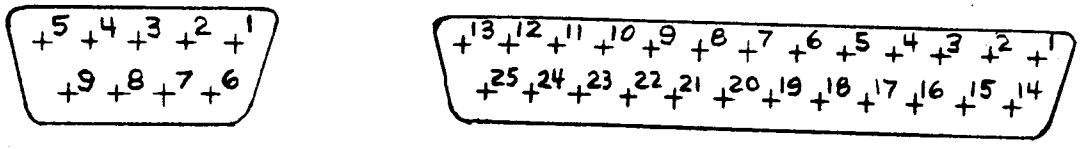


FIGURE 4-1 REMOTE CONNECTOR AND SERIAL ASCII CONNECTOR

SIGNAL	MNEMONIC	REAR PANEL REMOTE CONNECTOR PIN	SERIAL ASCII CONNECTOR PIN
BUS DATA	-BDATA	J11-3	
BUS DATA	+BDATA	-8	
BUS ON-TIME	-BON-TIME	J11-2	
BUS ON-TIME	+BON-TIME	-7	
BUS TIME SYNC	-BTSYNC	J11-1	
BUS TIME SYNC	+BTSYNC	-6	
ENABLE	ENABLE	J11-4	
GROUND	GND	-9	
TIME DATA	TDATA	J11-5	J4-19

BDATA, BON-TINE and BTSYNC signals conform to EIA RS-422 standard. TDATA conforms to RS-232C signal levels.

The +BON-TIME signal is a positive-going 0.1-second pulse relative to -BON-TIME, occuring once per second. The leading edge of the pulse is the beginning of the second.

The +BTSYNC signal is high relative to -BTSYNC after the NBS time code has been decoded. The signal goes low n minutes after the receiver has lost phase lock with the NBS signal. The number of minutes, n, that the signal stays active after the receiver has lost phase lock is selected by switch A1A2SW4-3,4. It remains low until another successful decoding is accomplished.

The ENABLE signal is +5 volts in series with 60 ohms.

Time information is broadcast in ASCII on BDATA and TDATA. A character consists of 1 start, 8 data, and 2 stop bits. Serial Data Structure is:

(CR)(LF)I(SPACE)(SPACE)DDD(SPACE)HH:MM:SS(SPACE)(SPACE)TZ=XX(CR)(LF)

where: I = space if clock set by WWVB (TIME SYNC lamp on)
* if clock set manually via RS-232 port
? if time sync lamp is off

DDD - Day of the year
HH:MM:SS = hours:minutes:seconds
XX = Time zone switch setting at rear panel

Output is UTC minus the time zone switch setting

Option 30 Fully Decoded Text Stream: This alternate data format can be furnished when the unit is purchased.

(CR)(LF)I(SPACE)WWW(SPACE)DDMMMYY(SPACE)HH:MM:SS(CR)(LF)

where: I = as defined above
WWW = day of week (MON, TUE, WED, etc.)
DD = numeric day of month (01 to 31)
MMM = month (JAN, FEB, MAR, APR, etc.)
YY= year without century (83, 84, 85, etc.)
HH:MM:SS = as defined above.

BUS IMPEDANCE - The source impedance is 120 ohms. At the far end of the bus terminate BDATA, BON-TIME, BTSYNC with 120 ohms connected across each twisted pair. Spectracom Bus Terminator part No. 016005 may be used.

CABLE - Twisted pair cable should be used for each of the signals.

4.2.2 OPTION 19 - PRINCIPLES OF OPERATION

This section discusses the circuits associated with Option 19, Remote Output Driver. The circuits associated with Option 19 are shown in Figure 2-2 Sheet 2. Figure 2-3 is the parts location drawing for the microprocessor board.

Option 19 adds a USART and a RS-422 driver to the microprocessor board. Day and time information is broadcast out once per second.

The on-time pulse IR0, interrupts the processor once per second. During this interrupt the processor initiates the transmission of time data to the USART. The USART performs a parallel/serial conversion and broadcasts the data on to the time bus via the RS-422 driver, U41 and RS-232C driver U42.

The first character, carriage return, follows the on-time pulse by less than 10 msec. The standard baud rate is 300. Higher baud rates may be selected by the Selectable Bit Rate switch A1A2SW2. Baud rates lower than 300 are too slow for the amount of data transmitted.

The Model 8171A 1PPS ON-TIME pulse is transmitted on the RS-422 time bus. This signal comes from A1A2U9-6 and is sent down the bus by A1A2U41. The signal is a positive-going once-per-second 100-millisecond pulse. It is synchronized to the on-time signal received from WWVB minus the setting of the path delay thumbwheel switch that is located on the rear panel.

The TIME-SYNC indicator is transmitted on the bus via A1A2U41. The signal will be high when the indicator is on and low when the indicator is off.

An ENABLE signal A1A2J10-7 comes from +5 volts through 60 ohms. Devices on the time bus may use this signal to enable their RS-422 receivers.

Ground is brought out on A1A2J10-8.

In summary, the processor is interrupted once-per-second by the on-time pulse. This initiates the transmission of the time data on the RS-422 bus and the RS-232C output. Other signals transmitted are the on-time pulse, time sync indicator, and enable signal.

4.2.3 OPTION 19 - PERFORMANCE CHECKS

This section contains maintenance information for Option 19. The test equipment required is an oscilloscope, a Spectracom Model 8173, and an RS-232C terminal.

TEST 1 - BDATA Connect an RS-232C terminal to the Remote Output via the Model 8173 or connect an RS-422 terminal directly to the Remote Output bus. The terminal will print/display the day of the year and time of day once per second.

If Option 30 is present, the day format will contain day of week, month, and year data.

TEST 2 - BON-TIME Using the oscilloscope observe the differential voltage between pin 7 and pin 2 on the Remote connector. The signal is a once-per-second 100-millisecond positive-going pulse greater than +2 volts in amplitude.

TEST 3 - BTSYNC On the Remote connector, observe the differential voltage between pin 6 and pin 1. When the Model 8171A Time Sync LED on the front panel is on, the differential voltage should be greater than +2 volts. When the Time Sync LED is off the voltage on pin 6 should be negative relative to pin 1 by a minimum of 2 volts.

TEST 4 - ENABLE With power on, the voltage at pin 4 should be +5 $\pm$0.5 volts.

TEST 5 - TDATA Monitor the TDATA output on pin 5 Remote output connector. The serial stream of data should be greater than $\pm$9 volts above and below ground. Monitor the same signal at pin 19 of the Serial ASCII connector.

These tests verify the proper operation of Option 19. If trouble is found, trace the signal back to the faulty IC, connector or component. Repair/replace and retest.

4.3.0 OPTION 23 - IRIG B OUTPUT

IRIG Option 23 provides the Spectracom Model 8171 WWVB Synchronized clock with an IRIG B Output. Both the BCD time code and Straight Binary Seconds, SBS, time code are provided.

The IRIG control function capability is not available on the Model 8171A.

Refer to Document 104-70 IRIG STANDARD TIME FORMATS published by the Range Commander's Council, White Sands Missile Range, August 1970 for details on the IRIG STANDARD TIME FORMATS.

4.3.1 OPTION 23 - SPECIFICATIONS

IRIG OUTPUTS: The IRIG code is brought out a rear panel BNC connector. The output is a TTL signal or an amplitude modulated signal. The selection is made by an internal switch. (SW 6)

TTL OUTPUT: TTL 50-ohm line driver (SN74S140).

AMPLITUDE MODULATED OUTPUT: A 1-KHz sine wave amplitude modulated by the time code. The open circuit output signal is a nominal:

MARK: 8 volts peak-to-peak
SPACE: 2.4 volts peak-to-peak

The output impedance is nominally 50 ohms and will drive a load of 600 ohms to ground.

4.4.2 OPTION 23 - INTERNAL SWITCHES

Switch A1A2SW6 TTL/AM, controls the signal applied to the IRIG output. In the TTL or ON position, the output signal is a TTL level. In the AM or off position, the signal is an amplitude modulated 1-KHz signal.

4.3.3 OPTION 23 - PRINCIPLES OF OPERATION

Figure 2-2 Sheet 7 is the schematic for the IRIG option. Figure 2-3 is the layout drawing for the microprocessor assembly A1A2.

The first section that will be described is the counter chain. The chain consists of 5 counters. Counter 0 in U44 divides the 1-MHz input on U44-9 by 10 and provides a 100-KHz output on U44-10. This signal is fed into counter 1 and 2 on pins U44-15 and U44-18. Counter 1 divides the 100 KHz input by 1000 to produce the frame element signal F_E (100 Hz). This signal interrupts the processor and causes the processor to output the next element to counter 2.

Counter 2 is programmed as a ONE-SHOT. The output at U44-17 drops at the beginning of the framing element and stays low for a period of 2, 5, or 8 milliseconds. This signal is inverted and amplified by U46, a 50-ohm TTL line driver. The signal is fed to the rear panel IRIG BNC connector via the TTL/AM select switch.

Counter 0 of U45 divides the 1 MHz input signal at U45-9 by 1000 to obtain the 1000-HZ carrier frequency at U45-10.

Counter 1 of U45 divides the 1-MHz input signal, U45-15 by 20 to obtain the 50-KHz clock frequency for the switched capacitor low pass filter U47.

The signals are synchronized to the ON-TIME pulse by U4, a one-shot. The output signal U4-4 is a negative-going 400 nanosecond pulse that is used to reset counters 0 and 1 of U44 and counter 0 of U45.

The output from counter 0 of U45 is a 1-KHz square wave. It is filtered by U47, a 4th order low pass switched-capacitor filter. The output from the filter is fed into the amplitude modulator. The modulator consists of operational amplifier U49 and analog switch U48. The analog switch is a single-pole double-throw switch which is controlled by the IRIG code. Feedback resistors R68 and R67 are selected by the switch. The output of the modulator is buffered by voltage follower U49 and fed to the rear panel IRIG BNC connector via a 51 ohm resistor and the TTL/AM select switch.

The code select switch in the lower left of the schematic selects the IRIG B code. The other positions are reserved for future code options. The outputs from the code select switch are fed to the processor via U20 Port B.

4.3.4 OPTION 23 - PERFORMANCE CHECKS

This section describes verification tests for Option 23.

Table 4-1 lists the recommended test equipment for checking the operation of the IRIG Option.

TABLE 4-1 RECOMMENDED TEST EQUIPMENT

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
Oscilloscope	2 Channel	Tektronix Model 455
Time Code Reader	Read IRIG B Code	Datum Systron-Donner

The test set-up is shown in Figure 4-2.

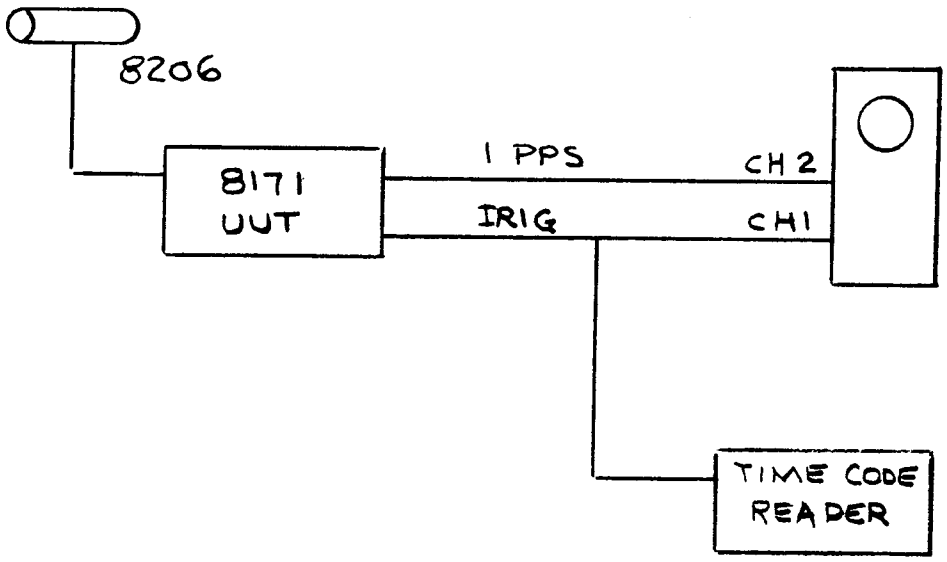


FIGURE 4-2 IRIG TEST SET-UP

Connect the Model 8171A WWVB Synchronized Clock to the Model 8161 and achieve Time Sync. Connect the IRIG output to channel 1 of a dual trace oscilloscope such as a Tektronix 455. Connect the 1 PPS output to channel 2. Synchronize the sweep to channel 2, 1 PPS and view the IRIG code on channel 1.

Connect an IRIG B Time Code Reader to the IRIG output. If control functions are present connect the CF inputs.

PERFORMANCE TESTS:

A. IRIG AM OUTPUT - With the TTL/AM switch A1A2SW6 in the OFF position, the output signal will be an amplitude modulated signal. The carrier frequency is 1 KHz and the mark to space ratio is typically 3.3 to 1.

V OUT MARK (7.2 - 9.0 V P-P) _____volts
V OUT SPACE (2.1 - 2.8 V P-P) _____volts

B. IRIG TTL OUTPUT - With the TTL/AM switch A1A2SW6 in the ON position, measure the IRIG TTL output signals.

V OUT HIGH (>2.7 volts) _____volts
V OUT LOW (<0.5 volts) _____volts

C. IRIG CODE WORD - Set the TTL/AM switch, A3SW6, to the ON position (TTL). Set the sweep speed at 5 milliseconds per division and synchronize the scope with the 1 PPS ON-TIME pulse. The scope will display the first 5 elements of the IRIG Code Word. The first element is 8 milliseconds in duration, the subsequent elements represent the least significant seconds bits.

Pulses will be 2 or 5 milliseconds wide.

Position Identifier (8 msec) _____
Weighted Code Digit (5 msec) _____
Unweighted Code Digit (2 msec) _____

D. READING THE TIME CODE - Connect a time code reader to the IRIG output. Verify that the BCD and SBS Code Words are correct.

BCD Code Word _____
SBS Code Word _____

4.4.0 OPTION 24 - TCXO AND EXTERNAL OSCILLATOR INPUT

Option 24 - Standby TCXO. A temperature compensated crystal oscillator provides the time base to the clock during signal loss, improving time error accumulation from about 1 second per day to about 0.01 seconds per day.

External Oscillator Input: Rear panel BNC input for 1.0 MHz standby clock oscillator. Maintains improved accuracy during signal loss. Standard on all Model 8171's.

4.4.1 OPTION 24 - SPECIFICATIONS

EXT 1-MHZ INPUT: This signal is AC coupled into 100-ohm terminating resistor. The minimum signal level is 1 V peak-to-peak and maximum is 10 V peak-to-peak. A BNC connector is used.

TEMPERATURE-COMPENSATED CRYSTAL OSCILLATOR, TCXO:

Temperature Stability 0°C to 50°C: $\pm 1 \times 10^{-6}$

Aging Rate: 5×10^{-7}/year, 3×10^{-9}/day average

Short-term stability 1×10^{-9}/second under constant conditions.

Frequency Adjustment: Sufficient to compensate for 5 to 10 years of aging.

Adjustment Resolution: $< 1 \times 10^{-7}$

Accuracy: Set at the factory to $\pm 1 \times 10^{-7}$

4.4.2 OPTION 24 - PRINCIPLES OF OPERATION

The time base for the Model 8171A WWVB Synchronized clock is normally derived from a voltage-controlled oscillator, which is located on the A2 board of the Model 8161, that is phase locked to the WWVB signal.

If the Model 8161 is disconnected from the Model 8171A, a 10-MHz crystal oscillator circuit internal to the Model 8171A runs the clock until the 8161 is reconnected.

Option 24 provides a Temperature-Controlled oscillator stand-by time base.

For discussion of operation, refer to Section 2.2, Microprocessor Assembly. The TCXO is located on Figure 2-2, Sheet 4.

4.5.0 OPTION 30 - FULLY DECODED TEXT STREAM

The standard unit outputs serial ASCII day and time information via the 25-pin series D RS-232C connector and, if Option 19 is present, via the 9-pin series D RS-422 data connector.

The standard unit data stream gives the day of the year, 1-366. Option 30 outputs the day of the week, day of the month, month of the year and the last two digits of the year, i.e. FRI27FEB84.

Adjusting the Time Zone switch on the rear panel will change the contents of the data stream.

The day-of-week and month is obtained algorithmically while the year data are read from two internal 10-position BCD switches. Switch A1A2SW3 sets the tens position of the year and A1A2SW1 sets the units position of year.

The algorithm that converts the day of the year to day-of-week and month-of-year is valid through the year 2010.

For details on the data structure, refer to Section 1.3.4 COMMANDS.

Option 30 data format is selected by placing switch A1A2SW4-2 in the ON position. To select the standard data format, place switch A1A2SW4-2 in the OFF position.

4.5.1 OPTION 30 - PRINCIPLES OF OPERATION

The Option 30 schematic is Figure 2-2, sheet 1. The assembly drawing is Figure 2-3.

Once per second the processor U1 converts the display day and time data from the standard format to the Option 30 format and adds the year information. The year data are read from switches A1A2SW1 and A1A2SW3. The Option 30 data is output on the RS-232C connector in response to a "T" command. See Section 1.3.4 COMMANDS for a description of the "T" command. If Option 19, Remote Output Driver is present, the Option 30 data stream is also fed out the Remote Output connector.

Switch A1A2SW4-2 Option 30 switch selects the standard data format if it is OPEN and the Option 30 format if it is CLOSED.

4.5.2 OPTION 30 - PERFORMANCE CHECKS

To verify the proper operation of Option 30, set the internal years switches A1A2SW1 (units) and A1A2SW3 (tens) to reflect the current year. Place switch A3SW4-2 in the ON position. Connect the Model 8161 and obtain time synchronization. Connect an RS-232C terminal and obtain the time printout by depressing "T" on the keyboard. The printout will give the current day of the week, month, and year.

transmitted. The electrical characteristics of the data signals conform to the EIA RS-422 standard. Up to 32 receivers may be employed at distances up to 4000 feet. If Option 30, Fully Decoded Text Stream, is present, the day of the week, month and year are transmitted. The day of the year (1-366) and TIME ZONE switch setting is not transmitted.

The Spectracom Model 8173 Multiple RS-232C Tap may be connected to the Remote Output bus. Model 8173 provides four RS-232C ports for easy interfacing to computer systems. Up to 32 Model 8173's may be connected to the bus.

An unlimited number of ports may be obtained by using the buffered output bus on the Model 8173. This port regenerates the data and provides another set of RS-422 drivers that can drive up to 32 loads at 4000 feet.

The Spectracom Model 8172 Remote Clock may be connected to Option 19 Remote Output Driver. Model 8172 is a digital wall clock that provides an HOURS, MINUTES, SECONDS 12- or 24-hour display.

The time data are also brought out as an RS-232C signal on both the Remote Output connector pin 5 and the Serial ASCII connector pin 19.

4.2.1 OPTION 19 - SPECIFICATIONS

Output Connector - The Remote Output Connector is a 9-pin series D receptacle (female). The Serial ASCII output connector is a 25-pin series D receptacle. Figure 4-1 shows the pin locations viewed from the rear of the Model 8171A.

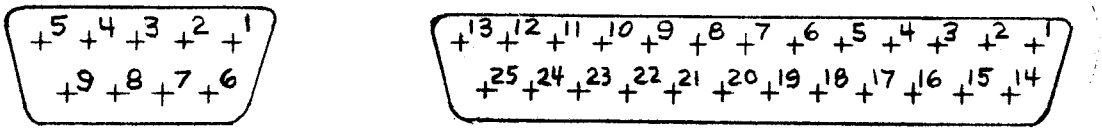


FIGURE 4-1 REMOTE CONNECTOR AND SERIAL ASCII CONNECTOR

The test set-up is shown in Figure 4-2.

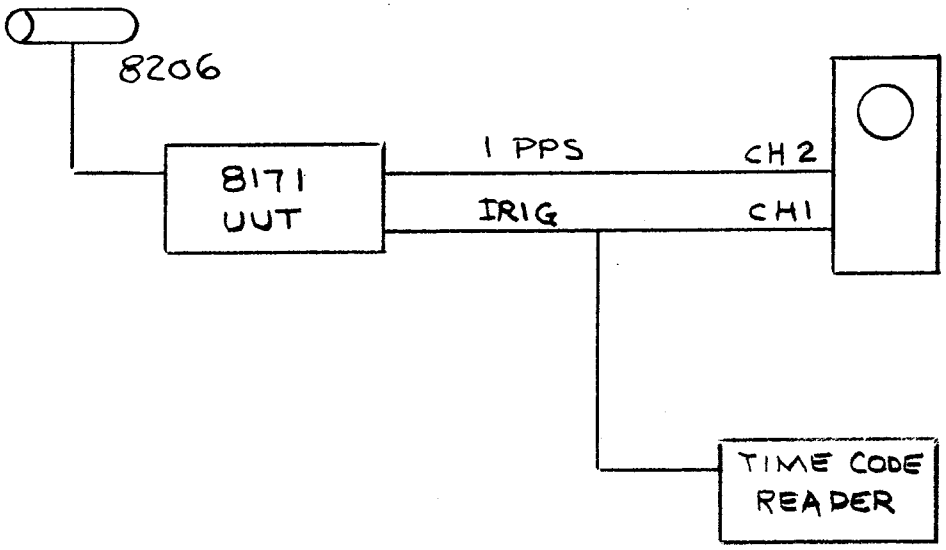


FIGURE 4-2 IRIG TEST SET-UP

Connect the Model 8171A WWVB Synchronized Clock to the Model 8161 and achieve Time Sync. Connect the IRIG output to channel 1 of a dual trace oscilloscope such as a Tektronix 455. Connect the 1 PPS output to channel 2. Synchronize the sweep to channel 2, 1 PPS and view the IRIG code on channel 1.

Connect an IRIG B Time Code Reader to the IRIG output. If control functions are present connect the CF inputs.

PERFORMANCE TESTS:

A. IRIG AM OUTPUT - With the TTL/AM switch A1A2SW6 in the OFF position, the output signal will be an amplitude modulated signal. The carrier frequency is 1 KHz and the mark to space ratio is typically 3.3 to 1.

V OUT MARK (7.2 - 9.0 V P-P) _____volts
V OUT SPACE (2.1 - 2.8 V P-P) _____volts

SECTION 5

REPLACEABLE PARTS LIST

REF. DESIGNATION	PART NO.	DESCRIPTION
FINAL ASSEMBLY		
F1	F00R75	Fuse, 3/4A 3AG
MAIN FRAME ASSEMBLY		
A1A1	015300	Power Supply Assembly
A1A2	015500	Microprocessor Assembly
A2A1	014100	Display Assembly
FRONT PANEL ASSEMBLY		
DS1	DS00045	Display, L.E.D
	DS00049	Lens, Green
	CA14013	Cable, 26 Conductor
SUBCHASSIS ASSEMBLY		
J1	J01000	Receptacle, AC Line
J3,4	J00010	Receptacle, BNC
J5	J00010	Receptacle, BNC - Option 23
J11	J03409	Receptacle, 9 pin - Option 19
	S00200	Nut Deco
S2	S00201	Switch, Toggle
S3	S00300	Switch, Thumbwheel
	CA14013	Cable, 26 Conductor
T1	T10000	Transformer, Power
XF1	X00050	Fuseholder
A1A1, POWER SUPPLY ASSEMBLY		
C1-4	C07222	Capacitor, Electrolytic, 2200 uf, 16V
C5	C09010	Capacitor, Electrolytic, 1 uf, 50V
C6	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C7	C07220	Capacitor, Electrolytic, 22 uf, 25V
C8,9	C09010	Capacitor, Electrolytic, 1 uf, 50V
C10,11	C08102	Capacitor, Electrolytic, 1000 uf, 35V
C12	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C13	C07220	Capacitor, Electrolytic, 22 uf, 25V
C14	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C15	C07220	Capacitor, Electrolytic, 22 uf, 25V
CR1,2	CR05624	Diode, 1N5624
CR3-6	CR05059	Diode, 1N5059
J1,2,4	J10014	Receptacle, 6 pin
W1-3	R01000	Jumper
U1	U78305	Voltage Regulator, 78T05 ACT
U2	U78M12	Voltage Regulator, 7812UC
U3	U79M12	Voltage Regulator, 7912UC
VR1	VR04735	Zener Diode, 1N4735A

REF. DESIGNATION	PART NO.	DESCRIPTION
A1A2, MICROPROCESSOR ASSEMBLY		
C1	C07220	Capacitor, Electrolytic, 22 uf, 25V
C2	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C5	C07220	Capacitor, Electrolytic, 22 uf, 25V
C6	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C7	C05560	Capacitor, Mica, 56 pf, 500V +-5% - Option 23
C8-12	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C13	C07220	Capacitor, Electrolytic, 22 uf, 25V
C14	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C15	C07220	Capacitor, Electrolytic, 22 uf, 25V
C16-22	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C23	C07220	Capacitor, Electrolytic, 22 uf, 25V
C24	C05301	Capacitor, Mica, 300 pf, 500V +-5%
C25	C05121	Capacitor, Mica, 120 pf, 500V
C26	C00040	Capacitor, Trimmer, 4.5-20 pf
C27	C05330	Capacitor, Mica, 33 pf, 500V
C28	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C29,30	C07220	Capacitor, Electrolytic, 22 uf, 25V
C31-37	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C38	C07220	Capacitor, Electrolytic, 22 uf, 25V
C39-42	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C43	C07220	Capacitor, Electrolytic, 22 uf, 25V
C44-46	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C47	C07220	Capacitor, Electrolytic, 22 uf, 25V
C48-56	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C57	C09010	Capacitor, Electrolytic, 1 uf, 50V
C58	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C59	C07220	Capacitor, Electrolytic, 22 uf, 25V
C60,61	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C62	C05301	Capacitor, Mica, 300 pf, 500V +-5%
C63,64	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C65	C09010	Capacitor, Electrolytic, 1 uf, 50V
C66-70	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C71	C05301	Capacitor, Mica, 300 pf, 500V +-5%
C72	C09010	Capacitor, Electrolytic, 1 uf, 50V - Option 23
C73,74	C26104	Capacitor, Ceramic, 0.1 uf, 50V
C101	C07220	Capacitor, Electrolytic, 22 uf, 25V
C102	C09010	Capacitor, Electrolytic, 1 uf, 50V
C103	C26104	Capacitor, Ceramic, 0.1 uf, 50V
CR2-8	CR00277	Diode, 1N277
E1,2	E02320	Terminal, Turret
J1	J06S50	Receptacle, 50 pin - Option 18
J2	J06S14	Receptacle, 14 pin
J3	J07S14	Plug, 14 pin
J4	J08025	Receptacle, 25 pin
J5	J02020	Receptacle, 20 pin
J6	J10014	Receptacle, 6 pin

REF. DESIGNATION	PART NO.	DESCRIPTION
A1A2, MICROPROCESSOR ASSEMBLY (continued)		
J7,9	J03213	Receptacle, 26 pin
J10	J02020	Receptacle, 20 pin - Options 19, 23
Q1	Q04124	Transistor, 2N4124
Q2	Q04258	Transistor, 2N4258
R1	R01103	Resistor, 1/4W, 5%, 10K
R2	R01122	Resistor, 1/4W, 5%, 1.2K
R3	R01104	Resistor, 1/4W, 5%, 100K
R4	R01103	Resistor, 1/4W, 5%, 10K
R5	R01560	Resistor, 1/4W, 5%, 56 ohm
R7	R01104	Resistor, 1/4W, 5%, 100K
R10	R01332	Resistor, 1/4W, 5%, 3.3K
R11	R01330	Resistor, 1/4W, 5%, 33 ohm
R12	R01393	Resistor, 1/4W, 5%, 39K
R13	R01153	Resistor, 1/4W, 5%, 15K
R14	R01151	Resistor, 1/4W, 5%, 150 ohm
R15	R01472	Resistor, 1/4W, 5%, 4.7K
R18	R01122	Resistor, 1/4W, 5%, 1.2K
R22,23	R01103	Resistor, 1/4W, 5%, 10K
R24	R01101	Resistor, 1/4W, 5%, 100 ohm
R26	R01000	Jumper
R29,30	R01101	Resistor, 1/4W, 5%, 100 ohm
R31	R01103	Resistor, 1/4W, 5%, 10K
R42	R01102	Resistor, 1/4W, 5%, 1K
R43	R01101	Resistor, 1/4W, 5%, 100 ohm
R44,45	R01562	Resistor, 1/4W, 5%, 5.6K
R46	R01102	Resistor, 1/4W, 5%, 1K
R47	R01472	Resistor, 1/4W, 5%, 4.7K
R48	R05103	Potentiometer, 10K
R49-51	R01102	Resistor, 1/4w, 5%, 1K
R52-56	R01121	Resistor, 1/4W, 5%, 120 ohm - Option 19
R57-59	R01103	Resistor, 1/4W, 5%, 10K - Option 23
R60	R01510	Resistor, 1/4W, 5%, 51 ohm - Option 23
R61	R01102	Resistor, 1/4W, 5%, 1K
R62	R01102	Resistor, 1/4W, 5%, 1K
R63	R01103	Resistor, 1/4W, 5%, 10K - Option 23
R64	R01472	Resistor, 1/4W, 5%, 4.7K - Option 23
R65-67	R01103	Resistor, 1/4W, 5%, 10K - Option 23
R68	R01333	Resistor, 1/4W, 5%, 33K - Option 23
R69	R01223	Resistor, 1/4W, 5%, 22K - Option 23
R70	R01183	Resistor, 1/4W, 5%, 18K - Option 23
R71	R01103	Resistor, 1/4W, 5%, 10K - Option 30
R72	R01361	Resistor, 1/4W, 5%, 360 ohm - Option 23
R105	R01103	Resistor, 1/4W, 5%, 10K
R106	R01224	Resistor, 1/4W, 5%, 220K
R112	R01103	Resistor, 1/4W, 5%, 10K - Option 23

REF. DESIGNATION	PART NO.	DESCRIPTION
A1A2, MICROPROCESSOR ASSEMBLY (continued)		
RP1-3	R36103	Resistor Network, 10K
RP4,5	R36561	Resistor Network, 560 ohm - Option 18
RP6	R36103	Resistor Network, 10K
RP7	R36561	Resistor Network, 560 ohm
RP8-13	R36561	Resistor Network, 560 ohm - Option 18
RP14	R36103	Resistor Network, 10K - Option 30
RP15	R36103	Resistor Network, 10K
SW1,3	S00320	Switch, 1 pole, 10 POS - Option 30
SW2	S00320	Switch, 1 pole, 10 POS
SW4	S00332	Dip switch, 4 SPST
SW5	S00320	Switch, 1 pole, 10 POS - Option 23
SW6	S00340	Dip switch, 1 SPST - Option 23
U1	U08085	Integrated Circuit, 8085A
U2	U4LS02	Integrated Circuit, SN74LS02
U3	U00555	Integrated Circuit, NE555
U4	ULS423	Integrated Circuit, SN74LS423
U5	U01489	Integrated Circuit, MC1489A
U6	U01488	Integrated Circuit, MC1488
U7	U4LS02	Integrated Circuit, SN74LS02
U8	ULS138	Integrated Circuit, SN74LS138
U9	U4S140	Integrated Circuit, SN74S140
U10	ULS138	Integrated Circuit, SN74LS138
U11	S00320	BCD Switch
U12	U08251	Integrated Circuit, 8251A
U13	U08259	Integrated Circuit, 8259A
U14	U4LS37	Integrated Circuit, SN74LS37
U15	U4LS90	Integrated Circuit, SN74LS90
U16	U07417	Integrated Circuit, SN7417 - Option 18
U17	U08255	Integrated Circuit, 8255A - Option 18
U18	U08755	Integrated Circuit, 8755A
U19	U08155	Integrated Circuit, 8155
U20	U08755	Integrated Circuit, 8755A
U21	U4LS04	Integrated Circuit, SN74LS04
U22	U4LS37	Integrated Circuit, SN74LS37
U23	U07417	Integrated Circuit, SN7417 - Option 18
U24,25	U08253	Integrated Circuit, 8253-5
U26	U4LS90	Integrated Circuit, SN74LS90
U27	U75175	Integrated Circuit, SN75175
U28-33	U07417	Integrated Circuit, SN7417 - Option 18
U34	ULS109	Integrated Circuit, SN74LS109
U35	U4LS04	Integrated Circuit, SN74LS04
U36	U75175	Integrated Circuit, SN75175
U37	U75174	Integrated Circuit, SN75174
U38	U4S132	Integrated Circuit, SN74S132
U39	U08755	Integrated Circuit, 8755A - Option 23

REF. DESIGNATION	PART NO.	DESCRIPTION
A1A2, MICROPROCESSOR ASSEMBLY (continued)		
U40	U08155	Integrated Circuit, 8155
U41	U6LS31	Integrated Circuit, AM26LS31 - Option 19
U42	U01488	Integrated Circuit, MC1488 - Option 19
U43	U08251	Integrated Circuit, 8251A - Option 19
U44,45	U08253	Integrated Circuit, 8253-5 - Option 23
U46	U4S140	Integrated Circuit, SN74S140 - Option 23
U47	U0MF10	Integrated Circuit, MF10 - Option 23
U48	U04053	Integrated Circuit, CD4053B - Option 23
U49	U00324	Integrated Circuit, LM324 - Option 23
VR1	VR04733	Zener Diode, IN4733A - Option 23
W	R01000	Jumper
X1	X00340	Integrated Circuit Socket, 40 pin
X3	X00308	Integrated Circuit Socket, 8 pin
X8, 10	X00316	Integrated Circuit Socket, 16 pin
X12,13	X00328	Integrated Circuit Socket, 28 pin
X17-20	X00340	Integrated Circuit Socket, 40 pin
X24,25	X00324	Integrated Circuit Socket, 24 pin
X39,40	X00340	Integrated Circuit Socket, 40 pin
Y1	Y00012	Crystal, 6.144 MHz
Y2	Y00011	Crystal, 10.000 MHz
Y3	015701	TXCO, 1 MHz - Option 24
A4, DISPLAY ASSEMBLY		
C1	C01104	Capacitor, Disc, 0.1 uf, 25V
DS1,2	DS00052	Display, L.E.D.
J1	J03213	Receptacle, 20 pin
R1,2	R01330	Resistor Metal, 1/4W, 5%, 33 ohms
U1-4	DS00072	7 Segment, Display, L.E D.
U5,6	DS00012	7 Segment, Display, L.E.D.
U7	U7218C	Display Driver, ICM7218C
ACCESSORIES ASSEMBLY		
	015504	Bus Terminator, Plug, 120 ohms
	015505	Bus Terminator, Receptacle, 120 ohms